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Development of

the BELLE Central Trigger System

Global Decision Logic

Yutaka Ushiroda

Department of Physics, Kyoto university

Abstract

In this paper, the design and development of components of the central trigger system of BELLE, called Global Decision Logic, is described, and their performances are reported. The role of Global Decision Logic is; receiving the informations from detectors at 1.85 μs after the event occurance, decides if it should be triggered, and if so, asserts the final trigger 2.2 μs after the event occurance. Since, till then, no one knows when was the event occurance, Global Decision Logic has to determine the time orgin, too. In order to make the trigger system flexible, each component is designed using programmable logic devices, and the logic is implemented actually and tested closely. Each module is found out to work as designed and also it is deduced that they will work as a whole.

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Chapter 1

Introduction

The violation of CP symmetry is a profound problem of particle physics. This CP violation is considered to be the origin of the fact that our universe is filled with matter, not with antimatter.

CP violation is first observed in the K meson system in 1964[1]. So far, the CP violation has not been observed in other systems yet. The Kobayashi-Maskawa theory explains the CP violation within the Standard Model, most plausibly. It predicts the presence of the direct CP violation, and a large CP violation in the B meson system.

Therefore, several so-called "B-factory" projects have been started in order to observe CP violation in the B meson system. The construction of two major B-factories, one at KEK and the other at SLAC, are going to be finished by the end of 1998. Since the typical branching ratio of the target decay mode which is usable for observation of CP violation is so small about $10^{-4} \sim 10^{-6}$, we need to generate many B mesons in order to get enough number of events of the mode. At KEK-B factory, 10^8 B mesons are generated in one year, observed by the BELLE detector, and the Kobayashi-Maskawa theory will be tested closely. To obtain so many B mesons, The KEK-B accelerator will run with full bunch and accomplish the luminosity $\sim 10^{34}$ cm^{-2} s^{-1}.

A key component to run the experiment at such high luminosity and high rate is the trigger system. The trigger system should be intelligent enough to distinguish the target decay modes of $B\bar{B}$ from backgrounds, as well as from the high rate events like Bhabha scattering etc, so that we can hold the trigger rate within the ability of the data acquisition system, without loosing

efficiency for target events. The BELLE trigger system consists of detector subtrigger systems and the central trigger system, called Global Decision Logic (GDL). Each detector subtrigger system generates its detector specific informations, and GDL unify them and assert the final trigger. So, GDL is the only responsible part to be intelligent.

In order to work with changeful condition of experiment, GDL is constructed using the technique of re-programmable logic devices like FPGA and CPLD. These are the fastest growing industries at persent. The aspect of trigger system has been changed by them drastically, and will be developed by them more and more in future, too. This paper reports the design, construction, and the performance of GDL. In chapter 2, the purpose of BELLE experiment is described. In chapter 3, the accelerator and the detector are summarized. In chapter 4, the whole picture of BELLE trigger system is described. In chapter 5, the data acquisition system of BELLE is briefly mentioned. The design of the Global Decision Logic is described in chapter 6, and its basic performance is reported in chapter 7. Finally, summary, conclusion and the prospects of future is given in chapter 8.

Chapter 2

Physics Motivation

2.1 Symmetries

There are many conservation laws of physics. These conservation laws are related to symmetries. In this section, the violation of two fundamental symmetries, parity (P) and charge conjugation (C), and their combinational symmetry (CP), are described.

2.1.1 Parity Transformation

Parity transformation changes the sign of spatial coordinate and does not change the sign of time coordinate, i.e.;

$$x = (t, \vec{x}) \rightarrow x_P = (t, -\vec{x}). \tag{2.1}$$

So the sign of spatial vector $\vec{x}$, momentum $\vec{p}$ are inverted. But the sign of angular momentum $\vec{L} = \vec{x} \times \vec{p}$, and spin $\vec{s}$ are not changed.

Parity transformation operator U_P can be written as,

$$\begin{aligned} \psi(x) \rightarrow \psi_P(x_P) &= U_P \psi(x) \\ &= e^{i\phi_P} \gamma^0 \psi(x). \end{aligned} \tag{2.2}$$

$e^{i\phi_P}$ is a phase factor.

Using the chiral representation of γ array:

$$\gamma^0 = \begin{pmatrix} \mathbf{0} & \mathbf{1} \\ \mathbf{1} & \mathbf{0} \end{pmatrix}, \boldsymbol{\gamma} = \begin{pmatrix} \mathbf{0} & -\boldsymbol{\sigma} \\ \boldsymbol{\sigma} & \mathbf{0} \end{pmatrix}, \gamma^5 = \begin{pmatrix} \mathbf{1} & \mathbf{0} \\ \mathbf{0} & \mathbf{-1} \end{pmatrix};$$

the spinor component of fermion field is,

$$\psi \equiv \begin{pmatrix} \xi \\ \eta \end{pmatrix}, \tag{2.3}$$

$$\psi_R = \frac{1+\gamma^5}{2}\psi = \begin{pmatrix} \xi \\ 0 \end{pmatrix} \tag{2.4}$$

$$\psi_L = \frac{1-\gamma^5}{2}\psi = \begin{pmatrix} 0 \\ \eta \end{pmatrix}. \tag{2.5}$$

$$\tag{2.6}$$

These components are transformed as,

$$e^{i\phi_P}\gamma^0\psi = e^{i\phi_P}\begin{pmatrix} \mathbf{0} & \mathbf{1} \\ \mathbf{1} & \mathbf{0} \end{pmatrix}\begin{pmatrix} \xi \\ \eta \end{pmatrix} = e^{i\phi_P}\begin{pmatrix} \eta \\ \xi \end{pmatrix}. \tag{2.7}$$

Namely, ψ_R and ψ_L are exchanged. So, for Weyl fermions, the parity is not conserved, because it has only one of the spinor components.

2.1.2 Charge Conjugation Transformation

Charge conjugation transformation changes the signs of every kind of charges of particle like electric charge, isospin, strangeness, and so on. Or briefly, it changes particle to its anti-particle.

Charge conjugation operator U_C can be written as,

$$\psi \to U_C\psi = e^{i\phi_C}\psi^C = e^{i\phi_C}i\gamma^2\psi^* = e^{i\phi_C}i\gamma^2\gamma^0\bar{\psi}^T \tag{2.8}$$

$e^{i\phi_C}$ is a phase factor which can be different for field by field.

The spinor components of fermion field are transformed as,

$$e^{i\phi_C}i\gamma^2\psi^* = e^{i\phi_C}i\begin{pmatrix} \mathbf{0} & -\sigma^2 \\ \sigma^2 & \mathbf{0} \end{pmatrix}\begin{pmatrix} \xi \\ \eta \end{pmatrix} = e^{i\phi_C}i\begin{pmatrix} -\sigma^2\eta \\ \sigma^2\xi \end{pmatrix}. \tag{2.9}$$

Again ψ_R and ψ_L are exchanged. So, the charge conjugation is not conserved for Weyl fermions.

2.1.3 CP Transformation

Another important symmetry is time reversal (T). So far, there is no evidence which objects the invariance under the combined transformation CPT. Given CPT invariance, CP violation and T violation is equivalent. In the following sections, CP violation will be described.

CP symmetry is violated when there is a complex coupling constant. We can take a whole phase factor arbitrarily, but when we cannot make all of the coupling constants real, CP violation occurs.

CP violation can be observed as the difference of decay probability between one mode and its CP transformed mode. Only when there are two independent amplitude contribution to the probability, CP violation can be observed. Consider the mode $X \to Y$ which has two independent amplitude.

$$\begin{aligned} Amp(X \to Y) &= A_1 e^{i\delta_1} e^{i\phi_1} + A_2 e^{i\delta_2} e^{i\phi_2} \\ &= A_1 e^{i\delta_1} e^{i\phi_1} \left[1 + \frac{A_2}{A_1} e^{i(\delta_2 - \delta_1)} e^{i(\phi_2 - \phi_1)} \right], \end{aligned} \tag{2.10}$$

where $\delta_{1,2}$ are the strong phase which are independent of weak phase $\phi_{1,2}$. The decay probability is proportional to square of the absolute value of the amplitude.

$$|Amp(X \to Y)|^2 = A_1^2 \left[1 + \frac{A_2^2}{A_1^2} + 2\frac{A_2}{A_1} \cos(\delta_2 - \delta_1 + \phi_2 - \phi_1) \right] \tag{2.11}$$

For the CP transformed mode, weak phase changes its sign and strong phase does not.

$$|Amp(X^{CP} \to Y^{CP})|^2 = A_1^2 \left[1 + \frac{A_2^2}{A_1^2} + 2\frac{A_2}{A_1} \cos(\delta_2 - \delta_1 - \phi_2 + \phi_1) \right]. \tag{2.12}$$

So, the asymmetry arises,

$$\begin{aligned} Asym &\propto |Amp(X \to Y)|^2 - |Amp(X^{CP} \to Y^{CP})|^2 \\ &= -4A_2 A_1 \sin(\delta_2 - \delta_1) \sin(\phi_2 - \phi_1). \end{aligned} \tag{2.13}$$

Thus, to observe the violation, the mode has to have two independent amplitude, and both the weak phase and strong phase must be different between the two amplitude ($\delta_2 \neq \delta_1, \quad \phi_2 \neq \phi_1$).

2.2 CP Violation in Standard Model

In this section, B physics is descrived in Standard Model. Considering with $SU(3)_C \times SU(2)_L \times U(1)_Y$, the source of CP violation is the complex phase of Kobayashi-Maskawa (KM) matrix element.

2.2.1 Unitarity Triangle

The quark mass eignestates are not same as the weak eignestates, and relation of these bases was given for six quarks as the matrix. Its explicit parametrization was done by Kobayashi and Maskawa in 1973. So, the matrix, say V, is called as Kobayashi-Maskawa matrix:

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = V \begin{pmatrix} d \\ s \\ b \end{pmatrix}. \tag{2.14}$$

$$\begin{aligned} V &= \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \\ &= \begin{pmatrix} c_{12} & s_{12}c_{13} & s_{13}e^{-i\delta_{13}} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta_{13}} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta_{13}} & s_{23}c_{13} \\ s_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta_{13}} & -c_{12}s_{23} - s_{12}c_{23}s_{13}e^{i\delta_{13}} & c_{23}c_{13} \end{pmatrix} \quad (2.15) \\ &= \begin{pmatrix} 1-\lambda^2/2 & \lambda & \lambda^3 A(\rho - i\eta) \\ -\lambda & 1-\lambda^2/2 & \lambda^2 A \\ \lambda^3 A(1-\rho-i\eta) & -\lambda^2 A & 1 \end{pmatrix} \quad (2.16) \\ &= \begin{pmatrix} 0.9745 \sim 0.9757 & 0.219 \sim 0.224 & 0.002 \sim 0.005 \\ 0.218 \sim 0.224 & 0.9736 \sim 0.9750 & 0.036 \sim 0.046 \\ 0.004 \sim 0.014 & 0.034 \sim 0.046 & 0.9989 \sim 0.9993 \end{pmatrix} \quad (2.17) \end{aligned}$$

In (2.15), $c_{ij} = \cos\theta_{ij}$ and $s_{ij} = \sin\theta_{ij}$, with $i, j \in \{1, 2, 3\}$ generation labels. (2.16) is approximate parameterization suggested by Wolfenstein, where λ is the Cabbibo angle $\lambda \simeq s_{12} = 0.221 \pm 0.002$. (2.17) is the measured value.

From the unitarity of KM matrix,

$$V_{ij}^* V_{ik} = \delta_{jk}. \tag{2.18}$$

Especially from the equation of $j = b, k = d$, namely neutral B meson case,

$$V_{tb}^* V_{td} + V_{cb}^* V_{cd} + V_{ub}^* V_{ud} = 0. \tag{2.19}$$

This relation can be represented as a triangle, so called as the Unitarity Triangle, shown in figure 2.1. The three angles ϕ_i $(i = 1, 2, 3)$ are defined as,

$$\begin{aligned} \phi_1 &= \arg\left(\frac{V_{cb}^* V_{cd}}{V_{tb}^* V_{td}}\right) \\ \phi_2 &= \arg\left(\frac{V_{ub}^* V_{ud}}{V_{tb}^* V_{td}}\right) \\ \phi_3 &= \arg\left(\frac{V_{cb}^* V_{cd}}{V_{ub}^* V_{ud}}\right) \end{aligned}$$

The lengths of sides of this triangle are,

$$V_{tb}^* V_{td} \sim \lambda^3, \quad V_{cb}^* V_{cd} \sim \lambda^3, \quad V_{ub}^* V_{ud} \sim \lambda^3. \tag{2.20}$$

So, none of the angles ϕ_i is small.

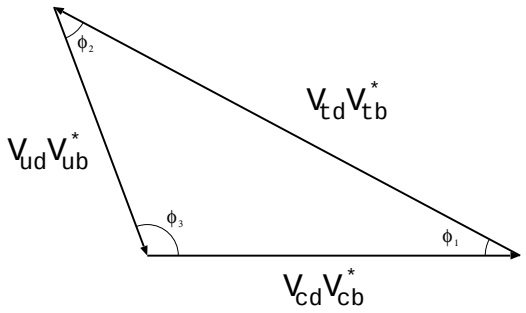

Figure 2.1: The Unitarity Triangle

On the other hand, by choosing other set of j and k in equation (2.18), we get other triangle. For example, for $j = s, k = d$,

$$V_{tb}^* V_{td} + V_{cb}^* V_{cd} + V_{ub}^* V_{ud} = 0, \tag{2.21}$$

which is neutral K meson triangle [Figure 2.2]. Lengths of sides are,

$$V_{ts}^* V_{td} \sim \lambda^5, \quad V_{cs}^* V_{cd} \sim \lambda^1, \quad V_{us}^* V_{ud} \sim \lambda^1. \tag{2.22}$$

So the angle between $V_{cs}^* V_{cd}$ and $V_{us}^* V_{ud}$ is quite small.

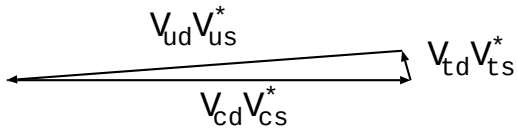

Figure 2.2: Unitarity Triangle for Neutral K Meson

This means in the B meson system, the CP asymmetry is larger than other mesons, like K meson. This is the reason why we choose B meson system to investigate. One of the main purpose of BELLE experiment is to measure the angles and the sides of the Unitarity Triangle. If it turns out not to be a triangle, it means that the Standard Model is wrong and there should be a new physics beyond the Standard Model.

2.2.2 Quantum Mechanics of B Meson System

The flavor eignestates, B^0 and $\bar{B}^0$, mix through the weak interactions (figure 2.3) and form the "light" and the "heavy" mass eigenstates B_- and B_+. In the following sections, this B meson system is described by quantum mechanics.

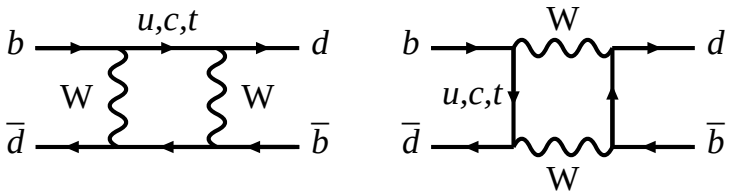

Figure 2.3: The box diagram for $b\bar{d} \leftrightarrow d\bar{b}$

Time Evolution of Neutral B Meason

B meson at the time t is written in the linear, orthonormal combination of $|B^0>$ and $|\bar{B}^0>$:

$$|B(t)>=\alpha(t)|B^0>+\beta(t)|\bar{B}^0>, \tag{2.23}$$

and it's time evolution is described by the Schrödinger's equation:

$$i\frac{d}{dt}|B(t)>=H|B(t)>, \tag{2.24}$$

or,

$$i\frac{d}{dt}\begin{pmatrix}\alpha(t)\\ \beta(t)\end{pmatrix}=\begin{pmatrix}<B^0|H|B^0> & <B^0|H|\bar{B}^0>\\ <\bar{B}^0|H|B^0> & <\bar{B}^0|H|\bar{B}^0>\end{pmatrix}\begin{pmatrix}\alpha(t)\\ \beta(t)\end{pmatrix}, \tag{2.25}$$

where

$$\begin{aligned} H &= M-(i/2)\Gamma \\ &= \begin{pmatrix} M_0-(i/2)\Gamma_0 & M_{12}-(i/2)\Gamma_{12} \\ M_{12}^*-(i/2)\Gamma_{12}^* & M_0-(i/2)\Gamma_0 \end{pmatrix}. \end{aligned} \tag{2.26}$$

Here, the diagonal elements are equal, supporsing the CPT invariance. Eigenvalues and eigenvectors are,

$$\lambda_\pm = M_0-(i/2)\Gamma_0 \pm \sqrt{(M_{12}-(i/2)\Gamma_{12})\,(M_{12}^*-(i/2)\Gamma_{12}^*)} \tag{2.27}$$

$$|B_\pm> = \frac{1}{\sqrt{|p|^2+|q|^2}}\left(p|B^0>\pm q|\bar{B}^0>\right), \tag{2.28}$$

where

$$\frac{q}{p}=\sqrt{\frac{(M_{12}^*-(i/2)\Gamma_{12}^*)}{(M_{12}-(i/2)\Gamma_{12})}}. \tag{2.29}$$

Define $M_\pm$ and $\Gamma_\pm$ as,

$$\lambda_\pm = M_\pm-(i/2)\Gamma_\pm, \tag{2.30}$$

and subtracting M_- from M_+, Γ_- from Γ_+, respectively,

$$\Delta M = M_+-M_-$$

$$
\begin{aligned}
&= Re.(\lambda_+) - Re.(\lambda_-) \\
&= 2Re.\left(\sqrt{(M_{12} - (i/2)\Gamma_{12})\,(M_{12}^* - (i/2)\Gamma_{12}^*)}\right) \qquad (2.31)\\
\Delta\Gamma &= \Gamma_+ - \Gamma_- \\
&= -2Im.(\lambda_+) - (-2)Im.(\lambda_-) \\
&= -4Im.\left(\sqrt{(M_{12} - (i/2)\Gamma_{12})\,(M_{12}^* - (i/2)\Gamma_{12}^*)}\right) \qquad (2.32)
\end{aligned}
$$

So,

$$\lambda_\pm = M_0 - (i/2)\Gamma_0 \pm \frac{1}{2}\left(\Delta M - (i/2)\Delta\Gamma\right). \qquad (2.33)$$

We can invert (2.28) as,

$$
\begin{aligned}
|B^0> &= \frac{\sqrt{|p|^2 + |q|^2}}{2p}\left(|B_+> + |B_->\right) \qquad (2.34)\\
|\bar{B}^0> &= \frac{\sqrt{|p|^2 + |q|^2}}{2q}\left(|B_+> - |B_->\right). \qquad (2.35)
\end{aligned}
$$

Consider the time evolution of the system which was $|B^0>$ at t=0. From (2.34),

$$
\begin{aligned}
|B^0(t)> &= \frac{\sqrt{|p|^2 + |q|^2}}{2p}\left(e^{-i\lambda_+ t}|B_+> + e^{-i\lambda_- t}|B_->\right) \qquad (2.36)\\
&= \frac{e^{-i\lambda_+ t}}{2}\left(g_+(t)|B^0> + \frac{q}{p}g_-(t)|\bar{B}^0>\right), \qquad (2.37)
\end{aligned}
$$

where

$$g_\pm(t) = 1 \pm e^{i(\Delta M - (i/2)\Delta\Gamma)t}. \qquad (2.38)$$

Ignoring $\Delta\Gamma t\,(\simeq \Delta\Gamma\cdot(1/\Gamma) \ll 1)$,

$$|B^0(t)> \simeq e^{-iM_0 t}e^{-\frac{\Gamma_0 t}{2}}\left[\cos\frac{\Delta M t}{2}|B^0> - i\frac{q}{p}\sin\frac{\Delta M t}{2}|\bar{B}^0>\right]. \qquad (2.39)$$

Similarly, the time evolution of the system which was $|\bar{B}^0>$ at t=0 is,

$$|\bar{B}^0(t)> \simeq e^{-iM_0 t}e^{-\frac{\Gamma_0 t}{2}}\frac{p}{q}\left[-i\sin\frac{\Delta M t}{2}|B^0> + \frac{q}{p}\cos\frac{\Delta M t}{2}|\bar{B}^0>\right]. \qquad (2.40)$$

$B^0 - \bar{B}^0$ mixing

From (2.39) and (2.40), the probability that the particle which was born at $t = 0$ as $B^0(\bar{B}^0)$ is observed at $t = t$ as $\bar{B}^0(B^0)$ is:

$$\begin{aligned} P[B^0 \to \bar{B}^0](t) &= \left| < \bar{B}^0 | B^0(t) > \right|^2 \\ &= e^{-\Gamma_0 t} \left| \frac{q}{p} \right|^2 \sin^2 \frac{\Delta M t}{2} \qquad (2.41) \\ P[\bar{B}^0 \to B^0](t) &= \left| < B^0 | \bar{B}^0(t) > \right|^2 \\ &= e^{-\Gamma_0 t} \left| \frac{p}{q} \right|^2 \sin^2 \frac{\Delta M t}{2} \qquad (2.42) \end{aligned}$$

Decay Rate to CP eigenstate

Since $|\Gamma_{12}| \ll |M_{12}|$, q/p can be approximated as,

$$q/p \approx \sqrt{M_{12}^*/M_{12}} \equiv e^{-2i\phi_M}, \qquad (2.43)$$

its absolute value $|q/p|$ can be approximated to 1. Thus, from (2.39) and (2.40), the decay rate of the B meson which was $B^0(\bar{B}^0)$ at t=0 to some CP eigenstate common to B^0 and $\bar{B}^0$, say, f_{CP} is,

$$\begin{aligned} &\Gamma \left[B^0(t) \to f_{CP} \right] \\ &= \int d\Gamma \cdot \frac{e^{-\left(\Gamma_0 + \frac{\Delta\Gamma}{2}\right)t}}{4} \left| g_+(t) \left\langle f_{CP} | B^0 \right\rangle + \frac{q}{p} g_-(t) \left\langle f_{CP} | \bar{B}^0 \right\rangle \right|^2 \\ &= \int d\Gamma \cdot e^{-\Gamma_0 t} \left| < f_{CP} | B^0 > \right|^2 \left| \cos \frac{\Delta M t}{2} - i \frac{q}{p} \rho \sin \frac{\Delta M t}{2} \right|^2 \\ &= \int d\Gamma \cdot e^{-\Gamma_0 t} \left| < f_{CP} | B^0 > \right|^2 \\ &\quad \times \left[\frac{1 + |\rho|^2}{2} + \frac{1 - |\rho|^2}{2} \cos \Delta M t + Im. \left(\frac{q}{p} \rho \right) \sin \Delta M t \right], \qquad (2.44) \\ &\Gamma \left[\bar{B}^0(t) \to f_{CP} \right] \\ &= \int d\Gamma \cdot e^{-\Gamma_0 t} \left| < f_{CP} | B^0 > \right|^2 \\ &\quad \times \left[\frac{1 + |\rho|^2}{2} - \frac{1 - |\rho|^2}{2} \cos \Delta M t - Im. \left(\frac{q}{p} \rho \right) \sin \Delta M t \right], \qquad (2.45) \end{aligned}$$

where

$$\rho \equiv \frac{< f_{CP}|\bar{B}^0 >}{< f_{CP}|B^0 >}, \quad \int d\Gamma : \textbf{integraloverphase space}.$$

Time-dependent asymmetries

From (2.44),(2.45), the time dependent CP asymmetry is given as,

$$\begin{aligned} & Asym\left[f_{CP}\right](t) \\ \equiv\ & \frac{\Gamma\left[B^0(t) \to f_{CP}\right] - \Gamma\left[\bar{B}^0(t) \to f_{CP}\right]}{\Gamma\left[B^0(t) \to f_{CP}\right] + \Gamma\left[\bar{B}^0(t) \to f_{CP}\right]} \\ =\ & \frac{1}{1+|\rho|^2}\left[2Im.\left(\frac{q}{p}\rho\right)\sin\Delta Mt - \left(|\rho|^2 - 1\right)\cos\Delta Mt\right]. \end{aligned} \quad (2.46)$$

2.3 Decay to CP eigenstate

There are so many decay channel in B meson that it's almost impossible to write about all of them. In this section, some major decay modes to CP eigenstate are introduced.

2.3.1 $J/\Psi K_s$

The decay mode $b \to c\bar{c}s$ is used to measure the angle ϕ_1. $J/\Psi K_s$ is a well-known CP eigenstate in this final state. Exactly saying, K_s is not a CP eigenstate. Yet, the CP violation in K meson system is rather small so that we can ignore it.

There're two large contributions for this decay; one is tree diagram (figure 2.4) and the other is penguin diagram (figure 2.5).

Contribution to the amplitude from the tree diagram is written as $V_{cb}^* V_{cs} A_t$.

Contribution from the penguin diagram is the sum of three terms, $(V_{ub}^* V_{us} + V_{cb}^* V_{cs} + V_{tb}^* V_{ts})A_t$. Ignoring $V_{ub}^* V_{us}$ in the unitarity relation $V_{ib}^* V_{is} = 0$, because $|V_{cb}^* V_{cs}|, |V_{tb}^* V_{ts}| \gg |V_{ub}^* V_{us}|$, we get $V_{cb}^* V_{cs} \approx -V_{tb}^* V_{ts}$. So the weak phase of amplitude of penguin diagram is approximately same as $V_{cb}^* V_{cs}$, namely that of tree diagram. So direct CP violation hardly occurs in this mode.

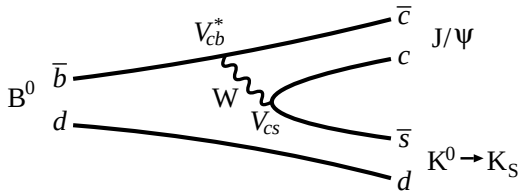

Figure 2.4: The Tree Diagram of $b \to c\bar{c}s$

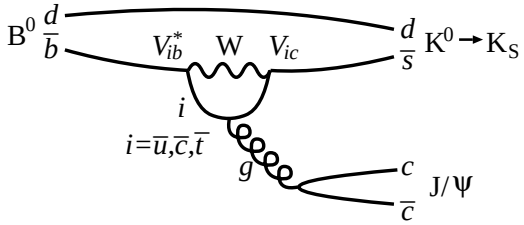

Figure 2.5: The Penguin Diagram of $b \to c\bar{c}s$

For this final state,

$$\begin{aligned} < J/\Psi K_s|B^0 > &= < K_s|K^0 >< J/\Psi K^0|B^0 > \\ &= \frac{p_K^*}{\sqrt{|p_K|^2+|q_K|^2}} V_{cb}^* V_{cs} A \qquad (2.47) \\ < J/\Psi K_s|\bar{B}^0 > &= \frac{q_K^*}{\sqrt{|p_K|^2+|q_K|^2}} V_{cb} V_{cs}^* A \qquad (2.48) \end{aligned}$$

So,

$$\rho = \frac{q_K^*}{p_K^*}\frac{V_{cb}V_{cs}^*}{V_{cb}^*V_{cs}}. \qquad (2.49)$$

By the way, the effective Hamiltonian[2] for the box diagram of $B^0 \leftrightarrow \bar{B}^0$ (figure 2.6) is, because the diagram with top quark in internal lines dominates over others,

$$H_B^{eff} = \frac{G_F^2 M_W^2}{4\pi^2}\eta_{QCD}^{tt} V_{tb}^* V_{td} V_{tb}^* V_{td} U(x_t, x_t)\bar{b}_L\gamma_\mu d_L + (h.c.), \qquad (2.50)$$

where

$$U(x,y) = \left[\frac{1}{4} + \frac{3}{2(1-x)} - \frac{3}{4(1-x)^2}\right]\frac{xy\ln x}{x-y} + (x \leftrightarrow y), \qquad (2.51)$$

and η^{tt} is the QCD correction [3], G_F is the Fermi coupling constant. So,

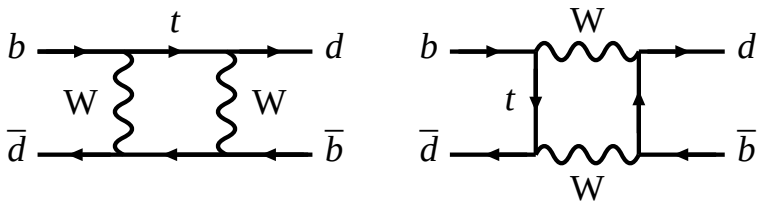

Figure 2.6: The box diagram for $B^0 \leftrightarrow \bar{B}^0$

$$M_{12} =< B^0|H_B^{eff}|\bar{B}^0 > \simeq \frac{G_F^2 M_W^2}{4\pi^2}\eta_{QCD}^{tt}(V_{td}^* V_{tb})^2 U(x_t,x_t) < B^0|\bar{d}_L\gamma_\mu b_L|\bar{B}^0 > . \qquad (2.52)$$

From (2.43),

$$\frac{q}{p} \simeq \frac{V_{td}V_{tb}^*}{V_{td}^*V_{tb}}. \tag{2.53}$$

On the other hand, the effective Hamiltonian for the box diagram of $K^0 \leftrightarrow \bar{K}^0$ (figure 2.7) is [4], because charm is dominant as the internal quark,

$$H_K^{eff} = \frac{G_F^2 M_W^2}{4\pi^2}\eta_{QCD}^{cc}V_{cs}^*V_{cd}V_{cs}^*V_{cd}U(x_c,x_c)\bar{s}_L\gamma_\mu d_L + (h.c.), \tag{2.54}$$

where η^{cc} is the QCD correction [5]. So, we get

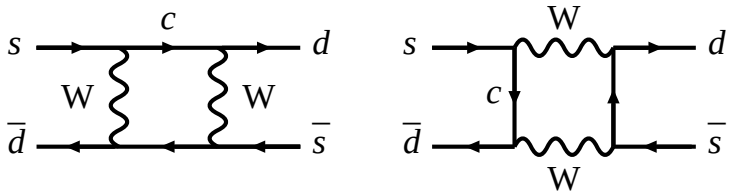

Figure 2.7: The box diagram for $K^0 \leftrightarrow \bar{K}^0$

$$\frac{q_K}{p_K} \simeq \frac{V_{cd}V_{cs}^*}{V_{cd}^*V_{cs}}. \tag{2.55}$$

Finally, from (2.46),(2.49),(2.53),(2.55), the time dependent CP asymmetry is,

$$\begin{aligned} Asym\left[J/\Psi K_s\right](t) &= \frac{1}{1+1^2}\left[2Im.\left(\frac{V_{td}V_{tb}^*}{V_{td}^*V_{tb}}\frac{V_{cd}^*V_{cs}}{V_{cd}V_{cs}^*}\frac{V_{cb}V_{cs}^*}{V_{cb}^*V_{cs}}\right)\sin\Delta Mt\right] \\ &= \sin\left(\arg\left(\frac{V_{td}V_{tb}^*V_{cd}^*V_{cb}}{V_{td}^*V_{tb}V_{cd}V_{cb}^*}\right)\right)\sin\Delta Mt \\ &= \sin\left(-2\arg\left(\frac{V_{cd}V_{cb}^*}{V_{td}V_{tb}^*}\right)\right)\sin\Delta Mt \\ &= -\sin 2\phi_1 \sin\Delta Mt. \end{aligned} \tag{2.56}$$

Thus, we can measure $\sin 2\phi_1$ through measuring the time dependent CP asymmetry of $B^0(\bar{B}^0) \to J/\Psi K_s$.

The branching fraction of $B^0 \to j/\Psi K^0$ is $(7.5 \pm 2.1) \times 10^{-4}$ [6].

2.3.2 $\pi\pi$

The decay mode $b \to u\bar{u}d$ is used to measure the angle ϕ_2. $\pi\pi$ is such final state with even CP.

The tree diagram of this mode is shown in figure 2.8, and,

$$< \pi\pi|B^0 >= V_{ub}^* V_{ud} A, \quad < \pi\pi|\bar{B}^0 >= -V_{ub} V_{ud}^* A. \tag{2.57}$$

So the time dependent CP asymmetry is, if the contribution is only from

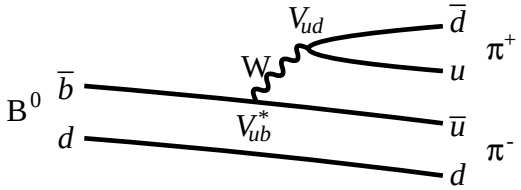

Figure 2.8: The Tree Diagram of $b \to u\bar{u}d$

this tree diagram,

$$\begin{aligned} Asym\,[\pi\pi]\,(t) &= Im.\left(\frac{V_{td}V_{tb}^*}{V_{td}^*V_{tb}}\frac{-V_{ub}V_{ud}^*}{V_{ub}^*V_{ud}}\right)\sin\Delta Mt \\ &= -2\sin\left(\arg\left(\frac{V_{td}V_{tb}^*}{V_{ub}^*V_{ud}}\right)\right)\sin\Delta Mt \\ &= -2\sin\phi_2\sin\Delta Mt. \end{aligned} \tag{2.58}$$

However, the contribution from the penguin diagram (figure 2.9) is not negligible to that of the tree diagram, because $V_{id}V_{ib}^* i = (u, c, t)$ are the same order of magnitude (2.20). Also, the weak phases of tree and penguin diagram are different, so the direct CP violation may occur.

It is possible, in principle, to disentangle the effects of the tree and penguin contributions for the final states $\pi\pi$, using isospin relations [7]. This method requires to measure the decay rate of $B^0 \to \pi^0\pi^0$, $B^0 \to \pi^+\pi^-$, and $B^+ \to \pi^+\pi^0$.

The branching fraction of $B^0 \to \pi^+\pi^-$ is less than 2.0×10^{-5} (CL 90%), $B^0 \to \pi^0\pi^0$ is less than 9.1×10^{-6} (CL 90%) [6].

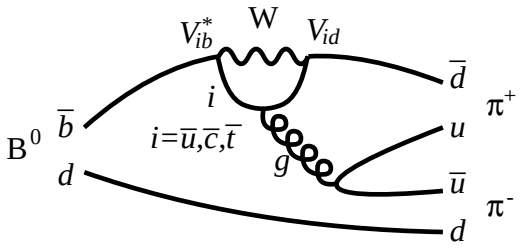

Figure 2.9: The Penguin Diagram of $b \to u\bar{u}d$

2.4 Tagging Decay

In order to observe CP asymmetry in neutral B mesons, as is shown in section2.3, it is necessary to measure the time-dependent decay ratio of neutral B mesons. So we have to know which B meson, $B^0(t)$ or $\bar{B}^0(t)$, decayed to a final CP eigenstate. Since a B^0 and a $\bar{B}^0$ which are created from a decay of $\Upsilon(4S)$ cannot be in the same flavor pair simultaneously, if we can know the flavor of either B meson, the flavor of another can be determined at the same instant of time. The method to know the flavor in the way explained above is called tagging.

There are several tagging decay modes; one example is high momentum lepton tagging. As is shown in figure 2.10, $B^0 \to X_{\bar{c}} l^+ \nu_l$ with 10.3 % branching ratio, on the other hand, $\bar{B}^0 \to X_c l^- \bar{\nu}_l$. Therefore the lepton charge indicates B meson's flavor.

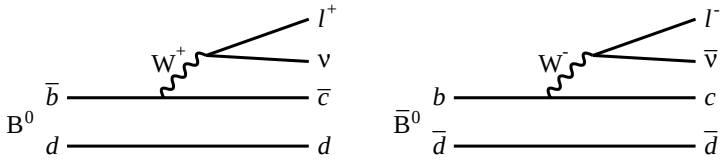

Figure 2.10: Lepton Tagging Decay

Chapter 3

B-factory

B-factory is an experimental facility to investigate the CP violation in the B meson system. There are many B-factory projects in the world. KEK B-factory is the one being built at KEK (High Energy Accelerator Research Organization, Japan). Both detector and accelerator construction have been excellently in progress.

3.1 KEKB accelerator

KEKB(figure 3.1) is an asymmetric electron-positron collider at 8×3.5GeV, in order to provide their collisions at a center-of-mass energy of 10.58Gev. Its aim is to produce $\Upsilon(4S)$s which decays into $B\bar{B}$ dominantly. The reason of energy asymmetry is to produce B mesons which are moving along the beam axis in the laboratory frame. Owing to its Lorentz boost, the proper lifetime of B meson gets longer and the time evolution measurement of B meson becomes more precise.

The cross-section of $\Upsilon(4S) \rightarrow B\bar{B}$ is 1.2 nb, and the typical branching ratios of interesting B meson decay modes are about 10^{-4} for 10^{-6}. We must get the integrated luminosity of some $100 fb^{-1}$, within the first one or two years, under competition with other B factory projects. So, the goal luminosity is $10^{34} cm^{-2} s^{-1}$. In order to achieve such high luminosity, 5,000 bunches are accumulated in each ring whose circumference is 3 km. Then, the bunch crossing rate will be 2 ns. In such high frequency operation, a bunch interacts with the next bunch through the RF cavities, and so called

"coupled bunch instability" phenomenon occurs. To avoid this, special cavity ARES (Accelerator Resonantly coupled with Energy Storage) is designed. The neighboring bunches also interact with each other via the residual gasses. This phenomenon is being studied now.

There is only one interaction point (IP) in the Tsukuba experimental hall, and there e^+ and e^- beams collide at an angle of ± 11 mrad. Owing to this finite angle, we don't need to bend the beam near the IP to separate e^- and e^+. This eliminates the synchrotron radiation background. So, another background due to beam-gas scattering is more harmful than the synchrotron radiation. The vacuum pressure in the IP section must be kept less than 10^{-9} torr.

The parameters[8] of KEKB is summarized in table 3.1.

3.2 BELLE detector

The BELLE detector[9][10] (figure 3.2) consists of seven detector components; SVD (Silicon Vertex Detector), CDC (Central Drift Chamber), ACC (Aerogel Čherenkov Counter), TOF/TSC (Trigger/Time of Flight Counter), ECL (Electo-magnetic Calorimeter), KLM (K_L and Muon detector) and EFC (Extreme Forward Calorimeter). 1.5 Tesla magnetic field is applied around the interaction region by a superconducting solenoid. KLM is outside of the solenoid and works also as a return yoke.

3.2.1 SVD

As is mentioned in section 2.4, we need to know the time between a tagging decay and a decay to CP eigenstate. So, we have to measure the decay points accurate enough to distinguish them as illustrated in 3.3. This is the requirement to SVD.

The SVD (figure 3.5, 3.4) has 3 layers, each one provides independent orthogonal two coordinate measurements with its double-sided silicon microstrips.

Table 3.1: Parameters of KEKB

1.without wigglers 2.with wigglers

Ring	LER	HER	
Energy (E)	3.5	8.0	GeV
Circumference (C)	3016.26		m
Luminosity (L)	1×10^{34}		$\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$
Crossing angle (θ_x)	± 11		mrad
Tune shifts (ξ_x/ξ_y)	0.039/0.052		
Beta function at IP (β_x^*/β_y^*)	0.33/0.01		m
Beam current (I)	2.6	1.1	A
Natural bunch length (σ_z)	0.4		cm
Energy spread (σ_E)	7.1×10^{-4}	6.7×10^{-4}	
Bunch spacing (s_B)	0.59		m
Particles/bunch	3.3×10^{10}	1.4×10^{10}	
Emittance ($\varepsilon_x/\varepsilon_y$)	$1.8 \times 10^{-8}/3.6 \times 10^{-10}$		m
Synchrotron tune (ν_s)	$0.01 \sim 0.02$		
Betatron tune (ν_x/ν_y)	45.52/45.08	46.52/46.08	
Momentum compaction factor (α_p)	$1 \times 10^{-4} \sim 2 \times 10^{-4}$		
Energy loss/turn (U_0)	$0.81^1/1.5^2$	3.5	MeV
RF voltage (V_c)	$5 \sim 10$	$10 \sim 20$	MV
RF frequency (f_{RF})	508.887		MHz
Harmonic number (h)	5120		
Longitudinal damping time (τ_ϵ)	$43^1/23^2$	23	ms
Total beam power (P_b)	$2.7^1/4.5^2$	4.0	MW
Radiation power (P_{SR})	$2.1^1/4.0^2$	3.8	MW
HOM power (P_{HOM})	0.57	0.15	MW
Bending radius (ρ)	16.3	104.5	m
Length of bending magnet (l_b)	0.915	5.86	m

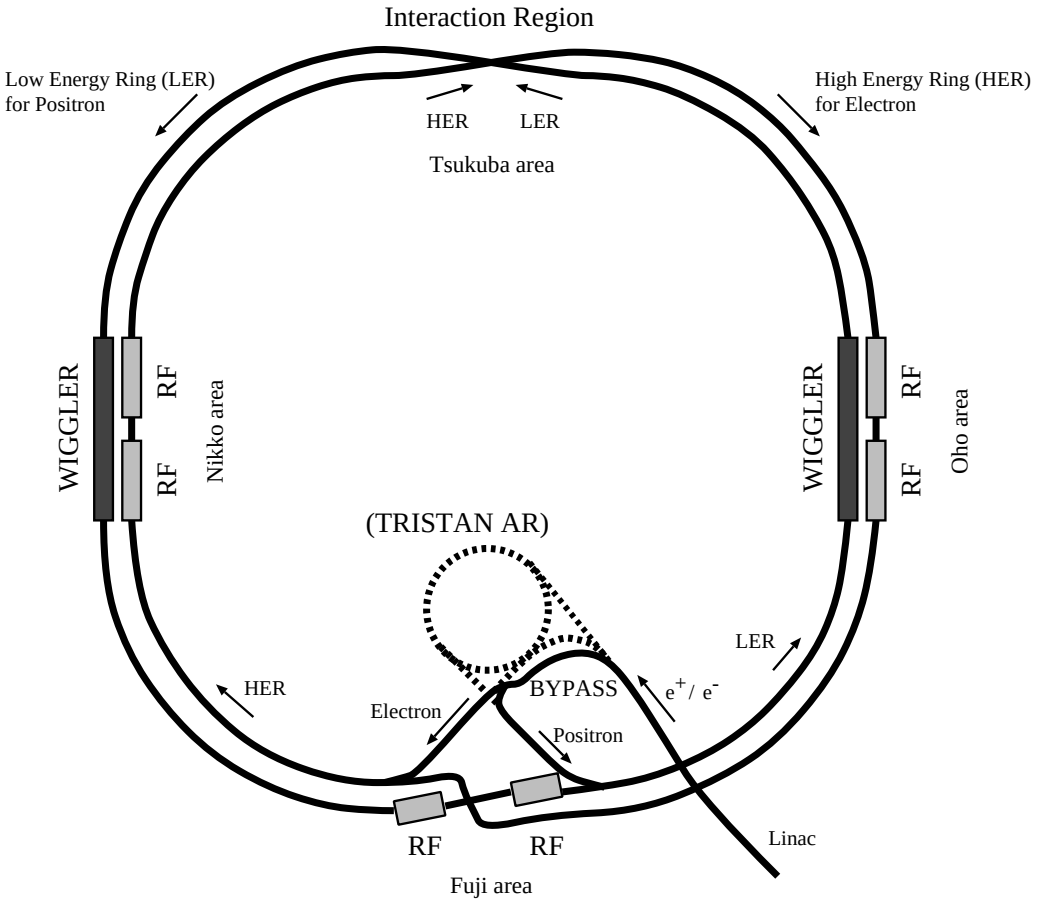

Figure 3.1: Configuration of the KEKB accelerator system

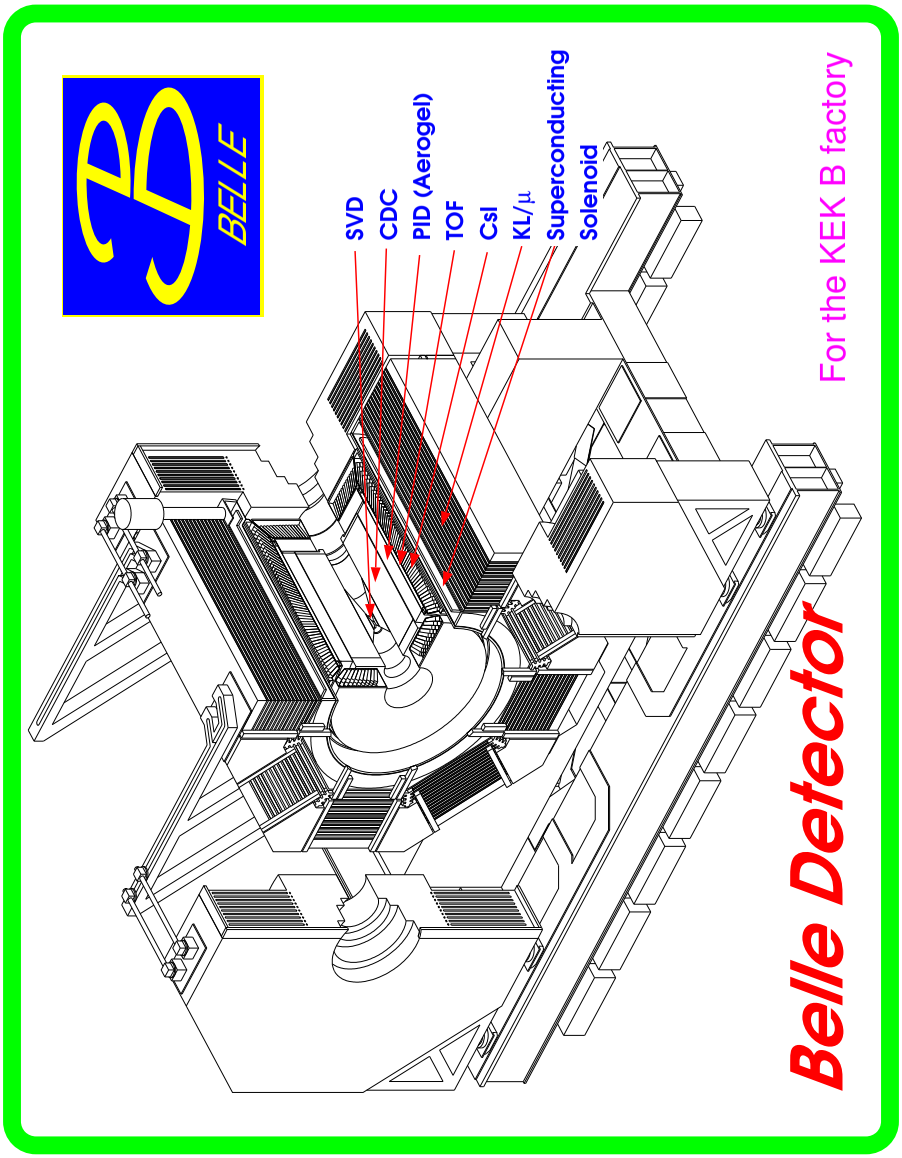

Figure 3.2: The BELLE detector

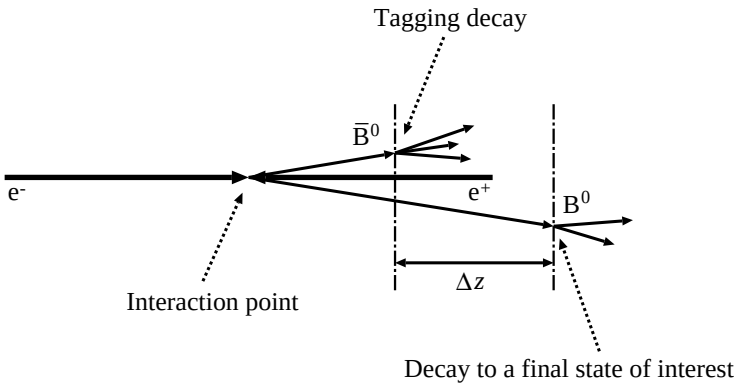

Figure 3.3: Propertime measurement

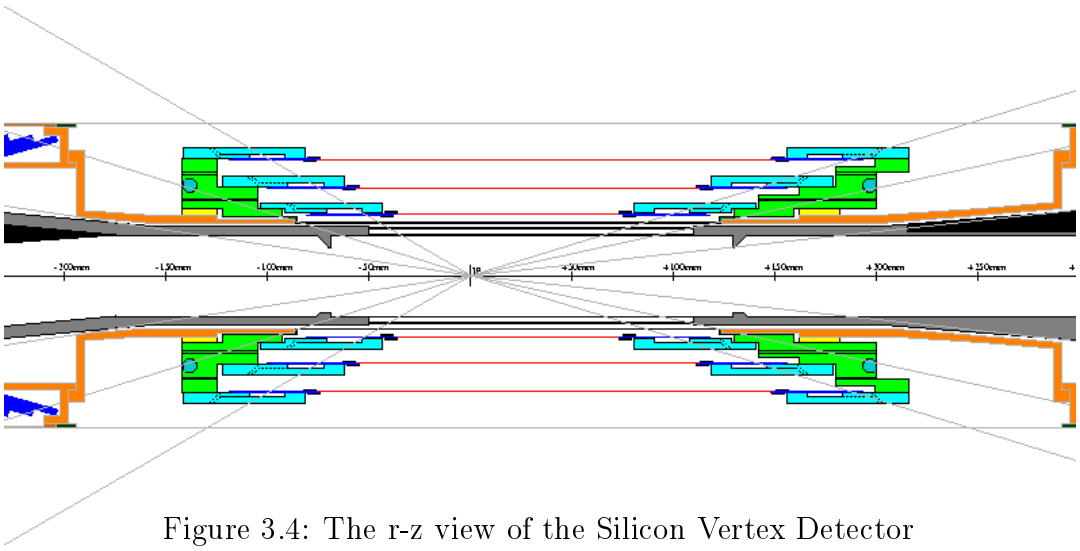

Figure 3.4: The r-z view of the Silicon Vertex Detector

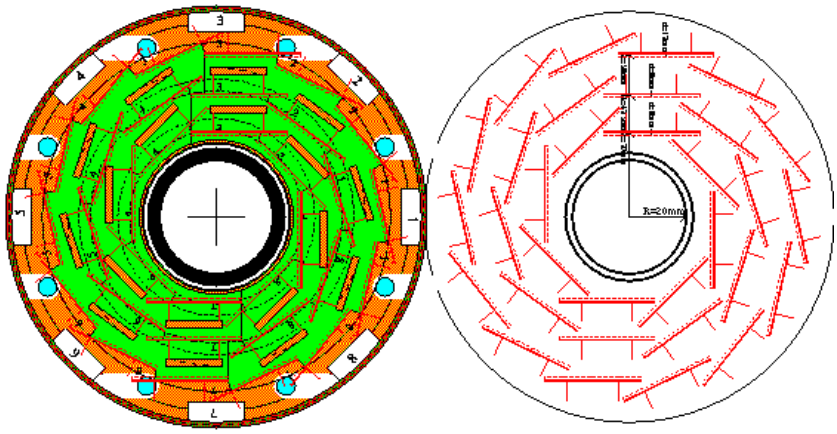

Figure 3.5: The r-ϕ view of the Silicon Vertex Detector

3.2.2 CDC

The purpose of the CDC is to give a high quality track information: momentum resolution σ_{p_t}/p_t is better than $0.5\%\sqrt{1+p_t^2}$,where p_t is the transverse momentum in GeV/c, for all charged particles that come to the polar angle region $17^\circ < \theta < 150^\circ$ with $p_t > 100MeV/c$; dE/dx resolution of 5% is expected.

The CDC structure consists of three parts (figure 3.6); the Cathode part which contains 3 sence wire layers and cathode strips; the Inner part which covers the region of the radius less than 28 cm with 10 layers; and the toroidally shaped Main part with 37 layers.

3.2.3 ACC

The ACC identifies particles with momentum more than 1.2 GeV/c, which is the limit of TOF, by catching Cherenkov radiations.

The ACC consists of a single layer of aerogel detectors, and is devided into two parts: the barrel part which occupies the region of $88.5cm < r < 115cm$ and $-85cm < z < 162cm$; and the forward endcap part which occupies $42cm < r < 114cm$ and $116cm < z < 194cm$; Figure 3.7 shows the barrel part.

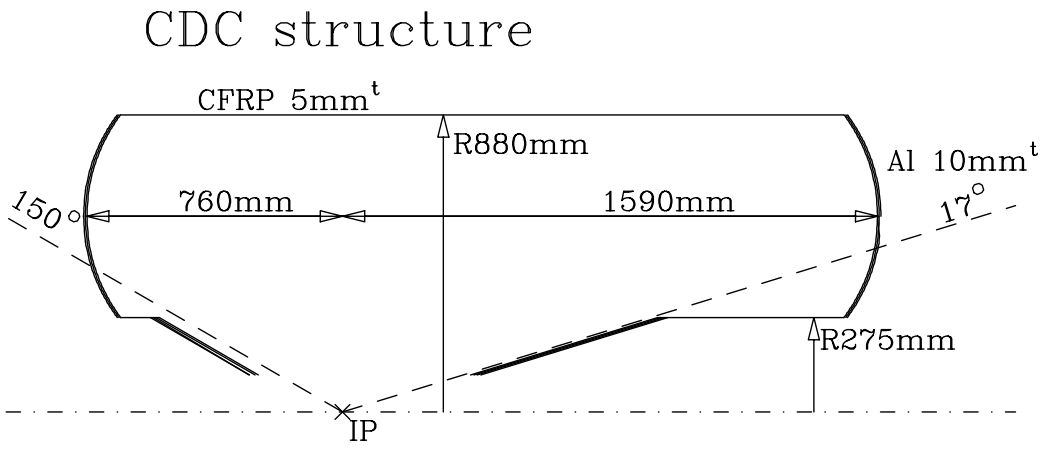

Figure 3.6: Structure of Central Drift Chamber

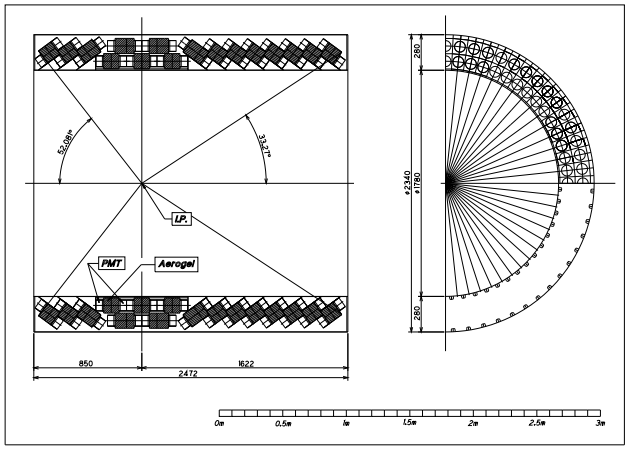

Figure 3.7: The Aerogel Čherenkov Counter

3.2.4 TOF/TSC

The TOF system identifies low momentum particles which do not radiate Cherenkov lights at ACC. It provides 3σ π/K separation up to 1.2 GeV/c with a TOF time resolution of 100ps. Taking the coincidence of TSC and TOF counters provides a clean timing signal for trigger.

The TOF/TSC system consists of 128 barrel TOF counters and 64 barrel TSC counters. Figure 3.8 illustrates one module of TOF/TSC.

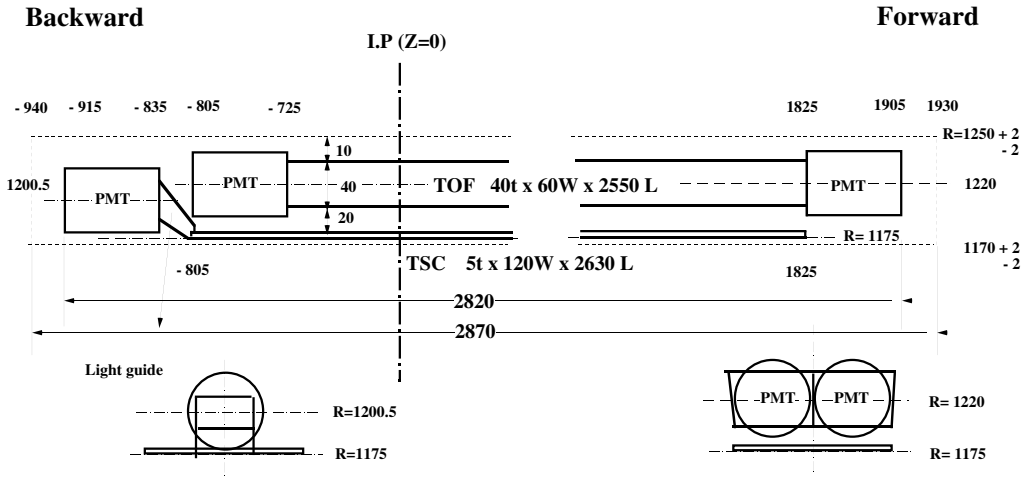

Figure 3.8: Time of Flight system

In the following sections, TOF and TSC are not distinguished, especially. TSC sometimes means the TOF/TSC system, representatively.

3.2.5 ECL

The main role of ECL is to measure the energies and positions of photons from B meson decay. Another role is electron identification. Electron identification is done by comparing the track momentum and the energy deposit on ECL. Besides, ECL provides the trigger timing for events which does not hit TSC.

CsI(Tl) crystal, whose typical size is around 6cm $\times$ 6cm $\times$ 30cm (actually, it is not unique), is chosen for the calorimeter. The configuration of ECL

is shown in figure 3.9. It consists of; the forward endcap, which covers the

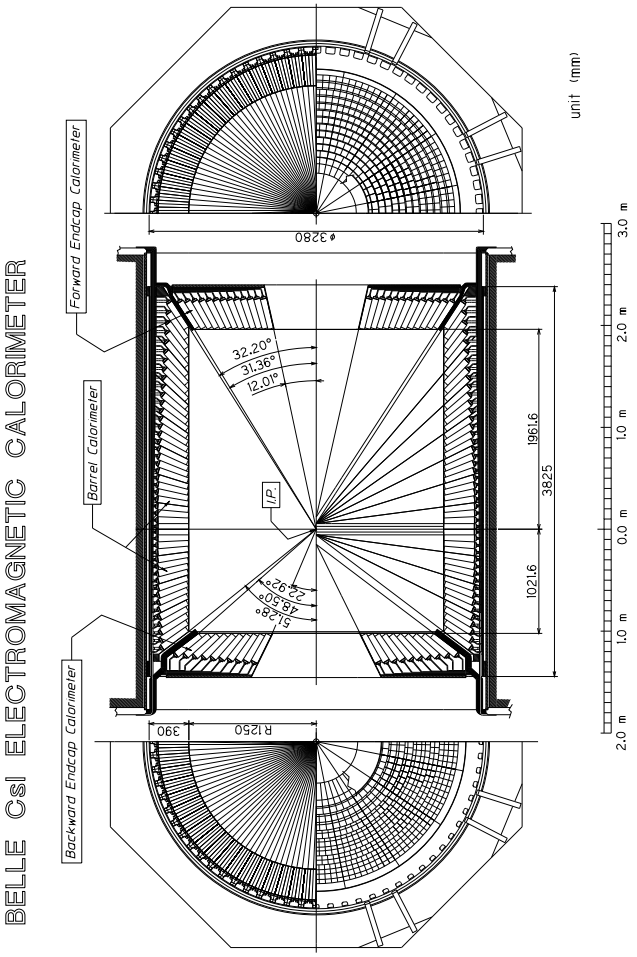

Figure 3.9: The Electro-Magnetic Calorimeter

region $12.4^\circ < \theta < 31.4^\circ$ with 1152 crystals, the barrel, $32.2^\circ < \theta < 128.7^\circ$ with 6624 crystals, and, the backword endcap, $130.7^\circ < \theta < 155.0^\circ$ with 960 crystals.

3.2.6 KLM

The KLM system distinguishes μ's and K_L's and measures their positions. It consists of octagonal barrel and two endcaps, composed of a sandwich of 14 iron plates of 4.4 cm thick each and 14 (15 for barrel part) layers of 4.7 cm thick RPC (Resistive Plate Counter). Note that the nuclear interaction length of iron is 16.8 cm and 14 $\times$ 4.4 cm thick iron corresponds to 3.68 interaction length. Figures 3.10, 3.11 are the barrel and endcap KLM detector, respectively.

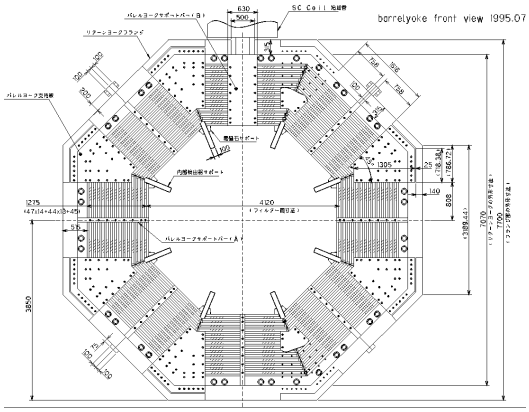

Figure 3.10: Front view of the barrel K_L and Muon Detector

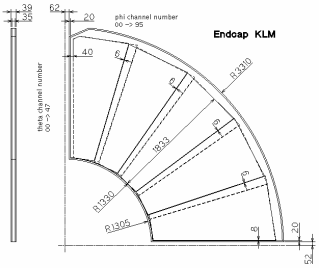

Figure 3.11: Front view of a quadrant of the endcap K_L and Muon Detector

3.2.7 EFC

The Extreme Forward Calorimeter (EFC) will be located close to the beampipe in order to detect particles at very small angles. One of the purposes of EFC is luminosity monitoring by measuring Bhabha scattering. Another purpose is tagging for two-photon process. These two processes have high event rate at small angle. Additional merit to put EFC is to increase solid angle coverage. EFC also reduces the probability of missing particles other than neutrino, and is helpful especially for the study of $B \to \tau\nu$, $B \to \pi l\nu$, etc. which has ν in the final state.

Chapter 4

Trigger system of BELLE

4.1 Overview

In BELLE experiment, we run at quite high luminosity like 10^{34} cm^{-2} s^{-1}, with almost continuous beam (bunch crossing rate : 500MHz), in order to see the physics of tiny event rate. So, the single rate at each detector end will be very high.

In such a situation, trigger must owe a big role and responsibility. The requirements to the trigger system are listed as follows:

1. High efficiency for all events of physics interest; especially $\simeq$ 100 % efficiency for $B\bar{B}$ events.

2. Redundant, independent triggers for important physics events; this will help to monitor the trigger efficiency for those modes.

3. Powerful reduction of background trigger rate to a tolerable level.

4. Sufficient flexibility to accomodate with varying beam condition. For the case that the background rate is higher than expected, the trigger rate should be reducible to the required level by applying more restrictive conditions without losing much efficiency for important physics events.

5. Facility of trigger rate monitoring, calibration, self-diagnostics.

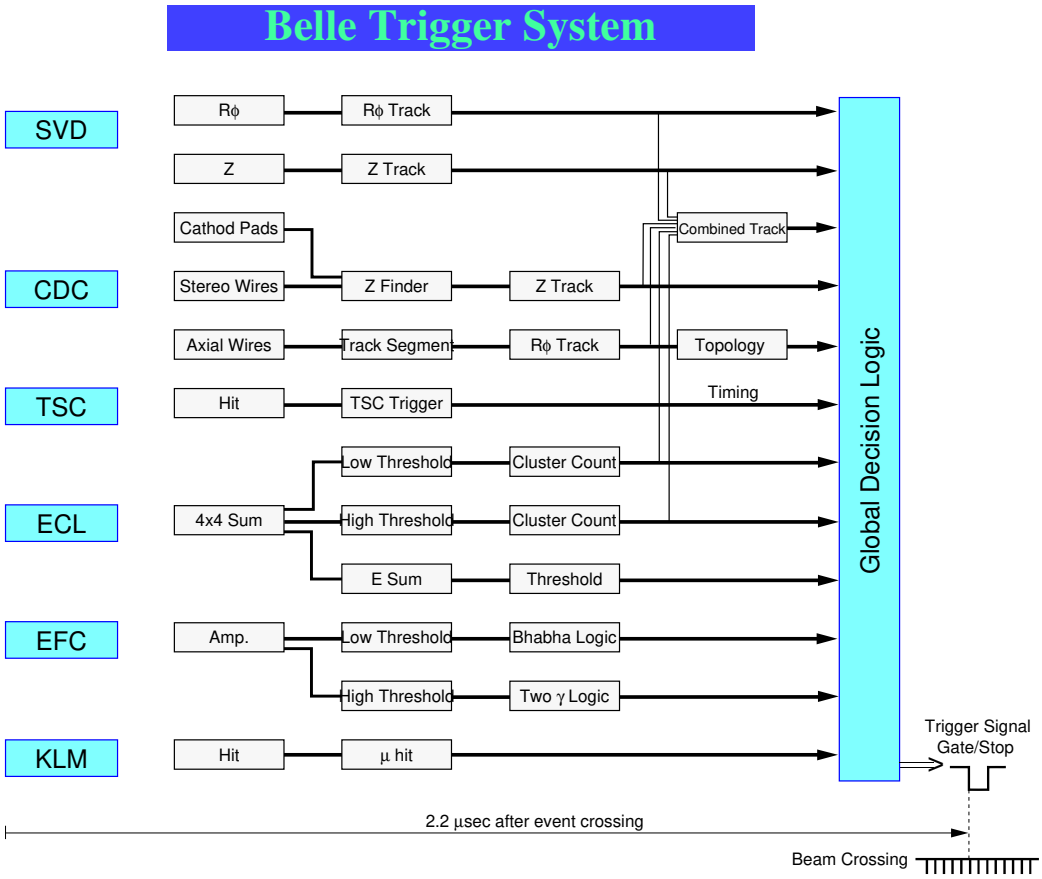

Figure 4.1: Schematic view of trigger system

BELLE trigger system is composed of detector sub-trigger systems and global decision logic. Figure 4.1 shows a schematic view of the trigger system.

Detector subtrigger systems are associated to each detector of BELLE, and pass its detector specific informations to global decision logic. They are CDC trigger, TSC trigger, and ECL trigger. SVD trigger, and KLM trigger are the future plan. Their details are described in section [4.2].

GDL gathers informations from those subtrigger systems so as to judge whether a physics event occurred or not. Especially owing to TSC trigger, it decides the event timing, and put out final trigger 2.2 μ sec after the event occurred. The final trigger timing 2.2 μs is decided from SVD DAQ subsystem. Analogue data of SVD is shaped so that the peak will come around 2.5 μs after the event occurrence. This peak is holded by the timing of final trigger. Slower shaping is possible, but unwanted, because increasing the shaping time, the number of background hits increases. If the timing of the final trigger is wrong, the peak cannot be holded properly, and correct pulse hight information cannot be obtained.

The final trigger starts the DAQ cycle. It is received by the sequence controller and distributed to each DAQ subsystems. Receiving the final trigger, DAQ subsystem starts digitizing the event data of the detector, and finishes within 200 μs. The data will be collected and stored by DAQ system. While the DAQ subsystems are busy for digitizing, the next trigger is blocked. Thus the dead time will be around 10% when the trigger rate is 500Hz. Details of the DAQ system are described in chapter 5.

One of the biggest issue for data acquisition is the trigger rate. Too high trigger rate will choke the DAQ system. So the trigger system must reduce the trigger rate so that the DAQ system can work safely with it.

In the full-bucket operation of KEK-B when the luminosity is expected to be $10^{34} cm^{-2} s^{-1}$, the trigger rate for physics processes will be $\sim$100 Hz. Details are described in the table 4.1. As noted in sections 2.3.1 and 2.3.2, the branching fraction of these interesting modes are about 10^{-5}. In the rate of 12Hz shown in the table, we get 10^8 $\Upsilon(4s) \rightarrow B\bar{B}$ decays in a year. Thus, we get about 10^3 events of such mode per year. When analyzing, some of the events are removed with backgrounds, therefore 12Hz is necessary to collect 100 events of such modes, and cannot be reduced due to, for example, trigger inefficiency.

On the other hand, the total background trigger rate is estimated to be $\sim$100Hz. This is due to cosmic ray background $\sim$20Hz, beam background

Table 4.1: total cross section and trigger rate

1. pre-scaled by factor 100
2. with restricted condition of $p_t \geq 0.3$ GeV/c

Physics Process	Cross Section (nb)	Rate (Hz)
$\Upsilon(4s) \rightarrow B\bar{B}$	1.2	12
Hadron production from continuum	2.8	28
$\mu^+\mu^- + \tau^+\tau^-$	1.6	16
Bhabha ($\theta_{lab} \geq 17^\circ$)	44	4.4[1]
$\gamma\gamma$ ($\theta_{lab} \geq 17^\circ$)	2.4	0.24[1]
2γ processes ($\theta_{lab} \geq 17^\circ$; $p_t \geq$0.2 GeV)	$\sim$15	$\sim$35[2]
Total	$\sim$67	$\sim$96

$\sim$50Hz and so on. Since the background estimation is not so exact, the trigger system must handle the case of higher background rate than expected, flexibly.

4.2 Trigger Subsystems

Detector subtrigger systems are classified as in the table 4.2.

Table 4.2: detector subtrigger systems

1.SVD, CDC, TSC, ECL etc. will be locally combined into TRK in future. 2.future plan

Track Trigger	TRK[1] SVD[2] TSC CDC
Calorimeter Trigger	ECL EFC
Timing Trigger	TSC ECL
Muon Trigger	KLM[2]

The roles of them are briefly summarized in the following sections.

4.2.1 Track Triggers

Track triggers select events based on the information of charged tracks. CDC trigger and TSC trigger are the source of track triggers. SVD trigger will be added in the future. For now, from TSC trigger, only the number of TSC hits[1] is passed to GDL as a track information, so it has just a supplemental role for Track triggers. In the future, information of TSC hit positions will also be passed to GDL via TRK. TRK is the subtrigger system planed for the future. It will collect detailed track information from SVD, CDC, TSC, and ECL, and give the combined information to GDL.

The SVD and the inner part of the CDC restrict the tracks to be close to the interaction point and have power to suppress cosmic ray backgrounds.

The $r-\phi$ hit patterns in the CDC are used to identify the track topologies and provide p_t information. The sub-trigger information given to GDL is listed in the table 4.3.

4.2.2 Calorimeter Trigger

The calorimeter is expected to generate trigger signals for hadrons, γ's and electrons/positrons from Bhabha events.

There're two kinds of triggers; a cluster-counting trigger and a total-energy trigger. The total energy trigger is sensitive to events with high electromagnetic energy deposit, while the cluster counting trigger is sensitive to events with minimum ionizing particles.

Identification of the Bhabha events is a very important role of calorimeter trigger. Bhabha events are prescaled by a factor $\simeq 100$ and used to measure the luminosity and to calibrate the detector responses.

The sub-trigger information given to GDL is listed in the table 4.4.

4.2.3 Timing Trigger

The main timing signal source for the final trigger is TSC. It has quite high efficiency for charged particles and its signal has very small jitter, so it's suitable for the timing trigger. However, these TSCs are not sensitive

[1]The reserved bits are to be used for a topological information, but they are only 2 bits.

Table 4.3: Track Triggers

1.future plan

2.track which goes through all CDC trigger layers;

$p_t \geq 300$ MeV/c and $30^\circ < \theta < 130^\circ$

3.track in the two innermost trigger layers;

$p_t \geq 200$ MeV/c and $17^\circ < \theta < 150^\circ$ and not full track

Detector	label	# of bits	comments
SVD[1]	N_{SVR}	2	# of SVD rϕ Track (N $= 1, 2, \geq 3$)
	N_{SVZ}	2	# of SVD Z Track (N $= 1, 2, \geq 3$)
	N_{SVRZ}	2	# of SVD r$\phi -$ Z Track (N $= 1, 2, \geq 3$)
CDC $r\phi$	$N_{CDR-full}$	2	# of CDC Full Track[2] (N $= 1, 2, \geq 3$)
	$N_{CDR-short}$	2	# of CDC Short Track[3] (N $= 1, 2, \geq 3$)
	CDC : B $-$ B	1	CDC Back to BackTracks
	CDC : open	1	maximum opening angle $>$ 90°
CDC Z	N_{CDZ}	2	# of CDC Z-track (N=1,2,$\geq$ 3)
TSC	N_{TSC}	2 + 2	# of TSC hits (N=1,2,$\geq$ 3) + reserve
TRK[1]	————	4	reserve

Table 4.4: Calorimeter Triggers

1.$E_1 = 1$ GeV $> E_2 > E_3$; the threshold values are changeable.

Detector	label	# of bits	comments
ECL	E_{tot}	3	$E_{tot} > E_1, E_2, E_3$[1]
	N_{icl}	3 + 1	# of isolated clusters ($(0-7)$ + reserve)
	ECL : BB_{pre}	1	ECL Bhabha (prescaled)
	ECL : BB	1	ECL Bhabha (non prescaled)
	ECL : Cosmic	1	ECL Cosmic flag
EFC	EFC : BB	1	EFC Bhabha
	EFC : Tag	1 + 1	Tag for two photon + reserve

to neutral particles; besides, since TSC covers only the barrel part, it is inefficient for the event which has no charged particle in the barrel part. Thus we need another timing trigger source which has sensitivity also to neutral particles like γ's and π^0's and which covers the endcap part. ECL satisfies such requirements, and is used as the second timing signal. Since CsI(Tl) is chosen as the crystal of ECL, its timing signal would have large jitter, yet, still it is useful and necessary.

The sub-trigger information given to GDL is listed in the table 4.5.

Table 4.5: Timing Trigger

Detector	label	# of bits	comments
TSC	TSC:timing	1	Charged Timing Trigger
ECL	ECL:timing	1	Neutral Timing Trigger

4.2.4 Other Sub-Triggers

Some other subtrigger inputs to GDL are planed. One is Muon Trigger from KLM; this will provide a muon flag. This is useful for the cosmic ray veto and for CDC calibration using high momentum muons, etc. Another is calibration triggers, whose substance is just a pulser etc. Table 4.6 shows these subtriggers.

Table 4.6: Other Subtriggers

Detector	label	# of bits	comments
KLM[1]	MU	1	Muons
CALIB	CALIB	3	calibration triggers

[1]future plan

4.3 Central Trigger System – GDL –

The GDL, global decision logic, is the central trigger system of BELLE. Its role is to assert the final trigger decided from all information given by detector subtrigger systems. So it's the core of whole trigger system.

The GDL provides the final trigger signals 2.2 μs delayed from the actual event occurrence. The timing and width of the subsystem triggers are adjusted so that their outputs always cover the beam-crossing at 1.85 μs at the GDL input, providing 350 ns processing time in the GDL. (In the following sections, the orgin of time t (t=0) is defined as the moment of the event occurrence at the interaction point.)

Table 4.7 shows the expected arrival time of the subtriggers and their width.

Table 4.7: Timing Characteristics of Subtriggers

Subtrigger	Arrival at GDL [μs]	Signal Width [ns]
CDC $r\phi$	$0.7 \sim 1.2$	$64 \sim 600$
CDC z	$1.0 \sim 1.5$	$64 \sim 600$
ECL	$1.65 \sim 1.85$	~ 500
TSC	$0.5 \sim 1.8$ (programmable)	~ 64

Subtriggers fed into GDL are listed in each subtrigger system's sections. The GDL outputs will be described in chapter 6.

Chapter 5

Data Acquisition System of BELLE

The basic requirements to BELLE data acquisition system is,

- Maximum trigger rate 500Hz,
- Number of readout channels 143K,
- Data size per event 30KB/event,
- Maximum data transfer rate 15MB/sec[1] .

Here, the requirement of manageable trigger rate to DAQ system is much severer than the estimation in section 4.1. The 143K channels are distributed as shown in the table 5.1.

DAQ system is illustrated in figure 5.1. Main data flow starts from the detector sub-systems, through the event builder, online computer farm, and ends at mass storage system.

At the detector sub-system[2], the analog signals from each detector is converted to time information in some way like QTC. The final trigger asserted by GDL is distributed to each detector sub-system by the sequence controller. Receiving the final trigger , digitization by TDC is started. While digitizing, the sequence controller blocks the next trigger. Digitization time,

[1]There's an upgrade plan to 30MB/sec.

[2]Exactly speaking, the way described here is not for all sub-systems.

Table 5.1: DAQ channel quota

Detector	No. of chs
SVD	85K
CDC	10K
ACC	2K
TOF	0.5K
ECL	10K
KLM	32K
EFC	0.3K
Trigger	3K
total	142.8K

which is expected to be less than 200 μs, is the cause of dead time. The event data is packed detector-by-detector by local CPU and passed to the event builder. The event builder rearranges these detector-by-detector data into event-by-event data and passes to the online computer farm. The online computer farm is called as the "L3 trigger" because it can fillter out some unwanted events. It does not reduce dead time due to digitization, but it reduces the number of events stored in the mass storage system. The mass storage system is a cluster of magnetic tapes, which is capable to record 30TB/year. The data stored in the mass sotrage system is read out by offline computers and analized. In this sense, the mass storage system is the interface between the DAQ system and analysis system (offline computers).

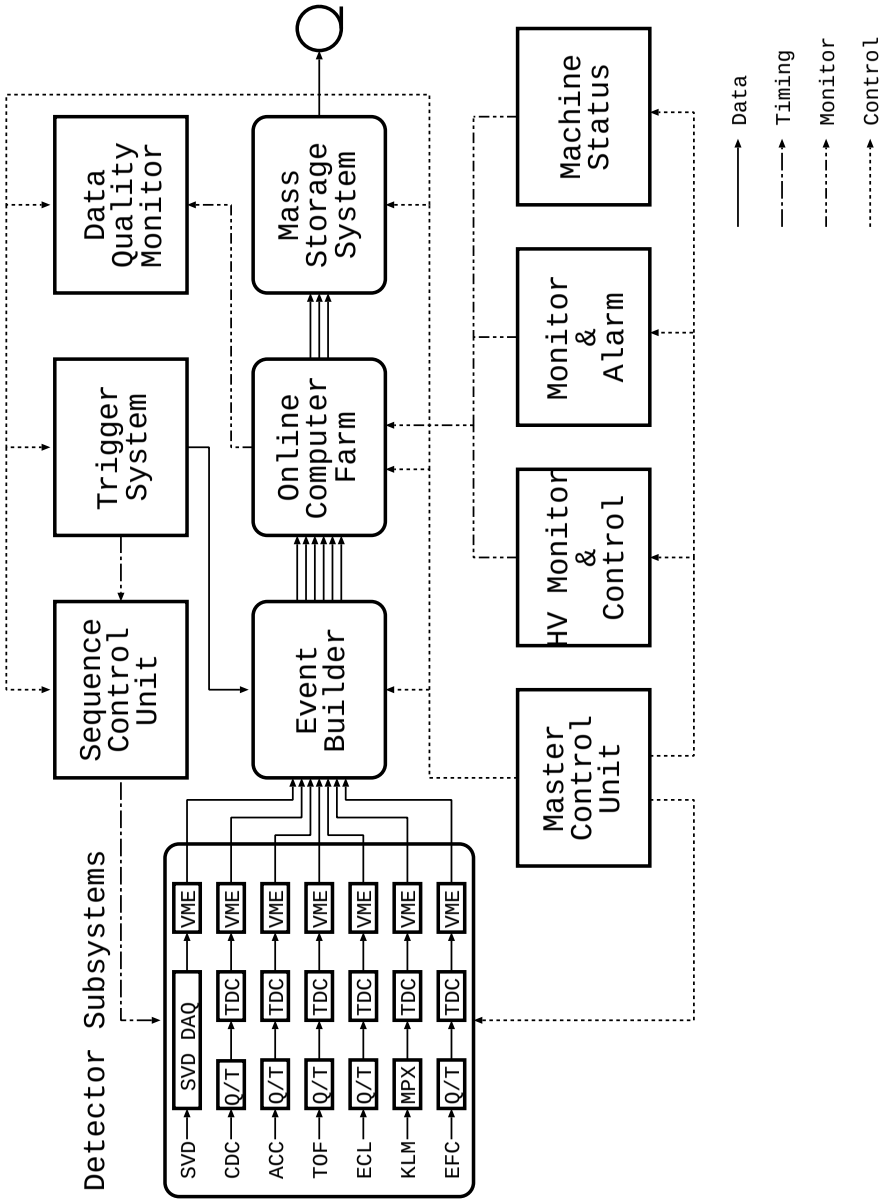

Figure 5.1: BELLE Data Acquisition System

Chapter 6

Construction of GDL

6.1 Introduction

The role of GDL (Global Decision Logic) is to make the final trigger decision using the information from the detector subtrigger systems, and to assert the final trigger at time t = 2.2 μs with accompanying trigger information. In short, there are two main roles; to judge whether the trigger should be asserted, and to decide the timing of the event occurrence. The final trigger is distributed by the sequence controller to every detector subsystems and starts the DAQ cycle. Trigger informations of GDL are monitored and recorded just in the same way as the data of detectors.

t < 1.85 μs is taken for the processing time of subtrigger systems, and the rest 350ns is for GDL. The timing 1.85 μs is limited by the processing time of the ECL subtrigger system (See table 4.7). 2.2 μs is limited by the peak hold timing of SVD DAQ. Since the final trigger is used to hold the peak at SVD and ECL DAQ, the jitter of the final trigger should be well small. If the peak hold time is improper, the measured charge will be incorrect, and the data loses reliability. Therefore the time plan of GDL is quite important.

Another important thing is tunability. In order to accommodate to the changeful requirement to trigger, the central trigger system should be flexible. For instance, at the first stage of experiment, we need to run the experiment in terrible beam backgrounds, then the trigger decision logic should be changeable to impose severer logic to reduce the background trigger rate; and when additional triggers are available from SVD, KLM and so on, the

trigger system should be easily expandable to treat these informations, too.

In order to accomplish the role, the task of GDL is divided into some function modules, and implemented into single width 6U VME modules. This division will help to construct, to control, to maintain, and to upgrade the system. VME is the most convenient currently available bus for high energy physics experiments, because of many commercially available on-board CPU's, interfaces to other buses. 6U crate is available in quite reasonable price and a board has enough room to implement each GDL function.

One prominent solution to meat the requirements – flexible logic and well-planned timing – is to use programable logic devices like FPGA's and CPLD's. These logic devices have upto several hundred thousands of gates and thousands of flip-flops in a chip. Connection between gates and flip-flops are in-system reprogramable. FPGA and CPLD are different in constitution, so we should use them properly to each module, according to their characteristics (see, appendix A).

Founding on such flip-flop-based system, the whole GDL processing is done synchronously with the GDL system clock which is made from the accelerator RF signal. The RF signal is 508.887 MHz; 8 pulses are grouped to produce 63.611 MHz clock, and 16 pulses are grouped to produce 31.805 MHz clock, and 32 pulses are grouped to produce 15.903 MHz clock. For simplicity, call these clocks as 64 MHz, 32 MHz, and 16 MHz clock, respectively. Basically 32 MHz clock is used for processing; 64 MHz clock is used only for the part concerning to the trigger timing, where better precision is required. Since the processing time of GDL is 350 ns, GDL will be 11 step pipe-line system, using 32MHz clock. The higher the system clock frequency is, the more difficult to make the system work synchronously. But with the lower system clock frequency, on the other hand, the lesser steps can be executed in the fixed 350 ns processing time. So, using 32 MHz clock seems the best and the only choice. For the trigger timing decision part, restriction to the system clock comes from the jitter requirement of final trigger and is inevitably decided as 64 MHz clock. So, subtle and attentive care should be taken to make that part.

6.2 Overview

Figure 6.1 is the schematic of whole GDL including its readout, monitoring etc. There are 10 kinds of modules, including those for test purpose.

First, the subtrigger signals from the detector subtrigger systems (total 48) are received by ITD (Input Trigger Delay) modules and adjusted their timings properly. All of them are passed to FTDL (Final Trigger Decision Logic). Two of them are the timing signals from TSC and ECL, and are also given to TMDL (Timing Decision Logic). FTDL checks their combinations, and only when the data satisfy the conditions for the events to be taken, it gives output, which indicates the characteristics of event (total 48). The outputs of FTDL are fed into PSNM (Prescaler and Mask Logic). Calibration and monitoring triggers are prescaled to give desired rates in PSNM. Unnecessary triggers can be masked out. PSNM outputs are ORed into 12 and fed into TMDL[1]. At TMDL, these 12 inputs are further ORed into one signal, which is the cue to start the timing decision. After TMDL receives this cue signal, it chooses the better timing signal out of the two which are from TSC and ECL. And according to the chosen timing signal, it asserts the final trigger at t = 2.2 μs, with the trigger type which indicates the chosen timing signal.

Figure 6.2 shows the timing chart of GDL processing. All subtrigger signals arrive at ITD before t = 1.85 μs and delayed properly (See section 6.3.4 for details). Define the clock 0 to 11 as in the figure. Before clock 1, ITD output will be valid at FTDL and latched by clock 1. FTDL tests the logic for the input (C = A & B in this example), and the consequence will be put out with clock 2. FTDL output will be latched by PSNM1 with clock3 and the output will be put out with clock 4. If PSNM's are cascaded, PSNM2 will latch the output of PSNM1 with clock 5 and put out with clock 6. The PSNM output is in time at TMDL, even if two PSNM's are cascaded, and latched as the cue signal. Then TMDL starts selecting the timing source, and asserts the final trigger with proper timing (22 64MHz clocks after TSC's arrival in case of this figure).

In order to read out the trigger data of GDL, TDC works as a LIFO

[1]Logically, these PSNM outputs can be ORed in the TMDL. But, a large number of locked pins decrease the degree of freedom of placement and routing inside the chip. Reducing the number of pins to be locked for input signals at the CPLD chip of TMDL helps to make a high speed system in the chip.

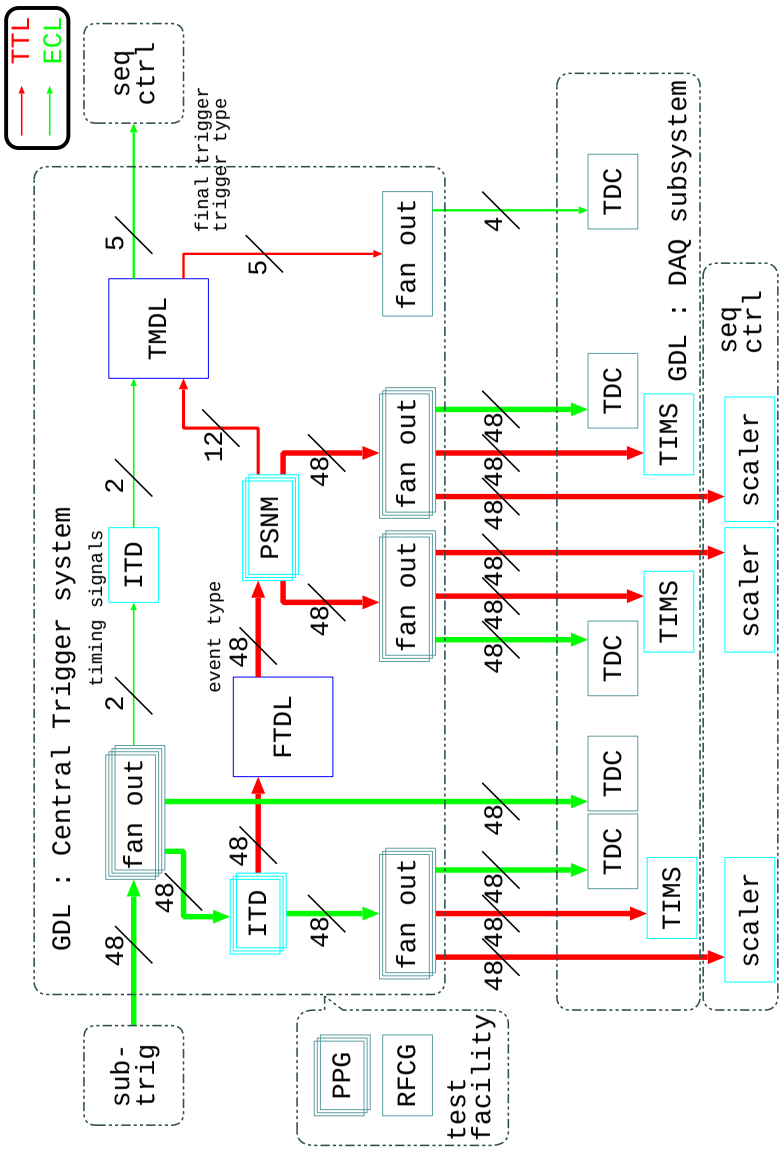

Figure 6.1: The entire scheme of Global Decision Logic

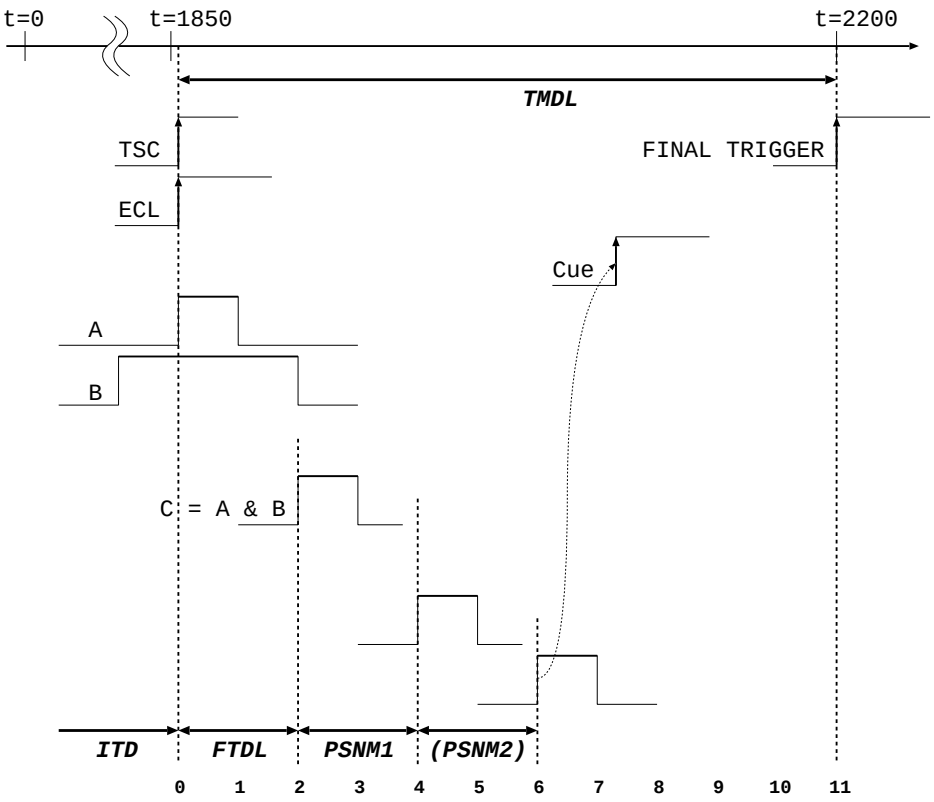

Figure 6.2: Timing Chart of Global Decision Logic : the numbers 0 to 11 are the tick of the system clock (32MHz).

buffer. TIMS is a FIFO based read out buffer module, which plays the same role as TDC. See the section 6.3.6 for these modules.

The scaler works in order to monitor the trigger rate and the dead time. Such monitoring facility is important for the diagnostic check on the trigger system. See the section 6.3.7.

PPG and RFCG is the self-test facility. GDL is checked *locally*, using the trigger pattern generated by PPG. In this paper, the performance measurement is done, using inputs from PPG. RFCG is the system clock source.

In the following sections, all GDL modules are described in detail.

6.3 GDL function modules

6.3.1 FTDL

The Final Trigger Decision Logic (FTDL) judges the event type from the input detector subtriggers listed in tables 4.3 to 4.6, and decides the event is wanted to be taken or not. Here, the event type means the every characteristics of event, like the number of tracks, the number of isolated clusters of ECL, and so on.

The width of the input signal (T_w^i) should satisfy the condition;

$$T_w^i = \Delta T_{max}^i + T_{clk}^{FTDL} + T_{margin},$$

where ΔT_{max}^i is the difference between the possible earliest and latest arrival time of the signal, T_{clk}^{FTDL} is the period of the FTDL system clock (31.442 ns) and $T_{margin} > 0$. This condition is imposed so that the input signal can cover the FTDL system clock at t = 1.85 μs everytime. Additional condition is imposed to a veto signal like ECL :BB and ECL:cosmic. They have to cover all the signals which are vetoed by them, so;

$$T_w^v \geq max.\{T_w^i + \Delta T_{max}^i\}$$

(see, figure 6.3). If the ECL subtrigger system cannot make veto signals satisfy this additional requirement, FTDL helps to enlarge the signal width.

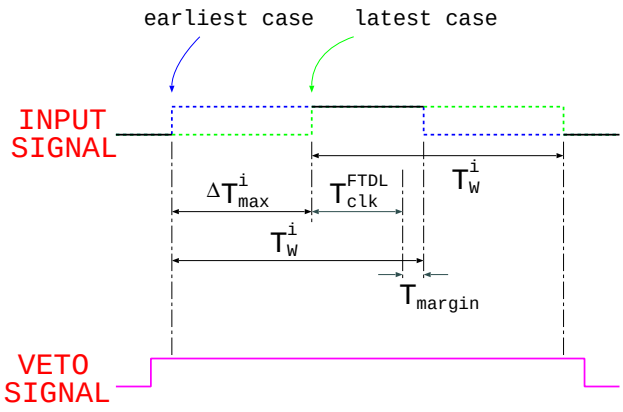

Figure 6.3: Requirement to the signals from Subtrigger System

logic The logic is basically just taking correlations between the inputs, so it can be represented as an array of AND, OR and NOT, and that part is to be changed according to the target of trigger. However, in the BELLE experiment, basic policy is to take every event from $B\bar{B}$ decay, so the correlation should not be biased so much. This gate array part is put in between two D flip-flops, in order to guarantee the simultaneity.

The table 6.1 shows an example of the correlations. Here, + means logical OR, $\times$ means logical AND and an overline means logical NOT.

hardware The FTDL module is designed, manufactured, and checked its performance (7.1). Its specification and feature is summarized as follows.

- Single width 6U VME module
- Total 96 TTL I/Os are received/transmitted through normal pitch[1] 17 pair flat cable connectors at the front panel; 48 are used for the inputs, the rest are for the outputs
- Two Xilinx CPLD's (XC95108-15PQ160 for logic part)
- Trigger Decision Logic is downloadable via VME bus

[1] 2.54mm pitch

Table 6.1: Final Trigger Decision Logic example
1.Prescaled at PSNM

output	correlation of inputs
Track Triggers	
Multi-Track:Rϕ	$(N_{CDR-full} \geq 3) + (N_{CDR-full} \geq 2) \times (N_{CDR-short} \geq 1)$
Multi-Track:RϕZ	$(N_{CDR-full} \geq 1) \times (N_{CDR-short} \geq 2) \times (N_{CDZ} \geq 1)$
Two-Track	$(N_{CDR-full} \geq 2) \times (N_{CDZ} \geq 1) \times$ $(N_{TSC} \geq 2) \times \overline{ECL:BB} \times$ CDC:open
Calorimeter Triggers	
E_{tot}	$(E_{tot} \geq E_1) \times \overline{ECL:BB} \times \overline{ECL:cosmic}$
Isolated Cluster	$(N_{icl} \geq 4)$
$E_{tot} \times$ ICN	$(E_{tot} \geq E_2) \times (N_{icl} \geq 3) \times \overline{ECL:BB}$
Bhabha Triggers	
ECL Bhabha	$ECL:BB_{pre}$
EFC Bhabha[1]	EFC:BB
Combinational Triggers	
Loose Track $\times$ E	$((N_{CDR-full} \geq 1) \times (N_{CDR-short} \geq 1)$ $+ (N_{CDR-short} \geq 2) \times (N_{CDZ} \geq 1)) \times (E_{tot} \geq E_2)$
Tag Two-photon	$((N_{CDR-full} \geq 2) + (N_{CDR-full} \geq 1) \times (N_{CDR-short} \geq 1)$ $+ (N_{CDR-short} \geq 2)) \times$ EFC:Tag $\times (N_{icl} \geq 2)$
Monitors	
Loose 2-Tracks[1]	$((N_{CDR-full} \geq 2) + (N_{CDR-full} \geq 1) \times (N_{CDR-short} \geq 1)$ $+ (N_{CDR-short} \geq 2)) \times$ (TSC:timing + ECL:timing) $\times \overline{ECL:BB}$
Single Track[1]	$(N_{CDR-full} \geq 1) + (N_{CDR-short} \geq 1)$
Low E_{tot}[1]	$(E_{tot} \geq E_3)$
Loose ICN[1]	$(N_{icl} \geq 2)$
Random	CALIB

- One NIM input through a lemo connector for the system clock
- Works with 32 MHz clock
- Consumes 2 clocks for processing
- Only one board is used in GDL.

See the appendix B.0.1 for more details.

6.3.2 PSNM

The Pre-Scaler and Mask Logic (PSNM) does, as its name stands, prescale or mask out the input signals, which are passed from FTDL. The prescale/masked outputs are given to the readout and monitoring systems (TDC, TIMS, Scaler), and the same signals, on the other hand, are ORed into 12 and given to TMDL. It also provides the fan out of input signals, in order to give the *FTDL outputs* to the readout and monitoring systems. This is required because we don't want to put Fan Out modules[1] in the main data flow, i.e. between ITD, FTDL, PSNM, and TMDL.

The modes to be prescaled are, as shown in the table 6.1, EFC Bhabha, Loose 2 Tracks, Single Track, Low E_{tot}, and Loose ICN. In the high energy physics experiment, to take a well-known, high rate event is quite important in order to check the detector and trigger efficiency. And to monitor such high rate event, we need to prescale in order to keep the total trigger rate around 200 Hz. Table 6.2 shows the estimated event rates[13] of the above modes and required prescale factors. These prescale factors are just crude estimations. Important thing is to limit the rate to several Hz.

logic It consists of a presettable synchronous counter and a register to store the prescale value, say p, for each channel. The counter counts the number of input signals fed in, and at the moment when the p-th signal arrives, the terminal count is set and put out. The counter (and the terminal count) is cleared by the trailing edge of the p-th signal. PSNM masks out when p is set to 0. See, the appendix B.0.2 for details.

[1] Because the fan out module has about 16ns propagation delay.

Table 6.2: Estimated Event Rate and Perscale Factors

Event Type	Rate	Prescale factor
EFC Bhabha	$1 \sim 2$ KHz	500
Loose 2 Tracks	280 Hz	90
Single Track	2.7 KHz	900
Low E_{tot}	~ 500 Hz(cosmic) +440 Hz(Bhabha) +300 Hz(beam background)	500
Loose ICN	~ 150 Hz(cosmic) +440 Hz(Bhabha) +1.5 KHz(beam background)	500

hardware PSNM is implemented on PLATO module, or so called Suehiro module [12],which was used as a level 2 trigger decision module in the KEK PS E162 (CP) experiment. The Suehiro module has four Xilinx FPGA chips (3190A), and each chip can hold four channels of prescale and mask logic. Specification is,

- Single width 6U VME module
- Total 64 TTL I/Os through normal pitch 17 pair flat cable connectors at the front panel; 16 are used for the inputs, 16 are used for the input signal fan out, 16 are used for the prescale/masked outputs, 4 are used for the ORed prescale/masked outputs.
- Four Xilinx FPGA (XC3190A)
- Two NIM input through lemo connectors for the system clock
- Operated with 32 MHz clock
- Consumes 2 clocks for processing
- 16 channels / board
- Prescale factor upto 255

- prescale factor is settable via VME
- counter is resettable via VME

See the appendix B.0.2 for more details. So far, the maximum prescale factor of one module is 255 and this is not enough for the modes listed in table 6.2. So, it is planned to cascade two modules[2] to reach the maximum prescale factor upto $255^2 = 65025$. This number seems enough even if the actual event rate turns out to be much more than the estimation. When cascading two, only the number which can be represented by a product of two numbers both less than 255 is possible as a prescale factor. But it does not do any harm. Important thing that happens when cascading two modules is that it requires extra two clocks. This is still manageable, since 1850 ns + 6 $\times$ 31.442 ns is well less than 2100 ns.

6.3.3 TMDL

The Timing Decision Logic (TMDL) asserts the final trigger at t = 2.2 μs with trigger type information which shows the source of the trigger timing described below. The inputs are timing signal from TSC, timing signal from ECL, and cue signal from FTDL-PSNM.

The timing signal should be adjusted its timing so that it arrives at TMDL at t = 1.85 μs in average. As a timing source, TSC is better than ECL because its jitter is much smaller than that of ECL (TSC$\sim$5ns, ECL$\sim$100ns). So TMDL checks if TSC timing signal has arrived or not, and only when there is not TSC signal but there is ECL signal, uses ECL signal as a source. Besides, for the case there is no timing signal from TSC or ECL, either, TMDL asserts the final trigger without timing signal source, i.e. only from the cue signal. Define the trigger type as,

0 : when its timing is decided from TSC timing signal,
1 : when decided from ECL timing signal,
2 : when decided just from the cue signal.

Note that the timing precision is less than one 64 MHz clock period in case of type 0, around 100 ns in case of type 1, and not at all precise (around 500 ns) for type 2.

[2]There's an optional plan to increase the max prescale factor of one board.

This back-up facility is necessary because there're some events possible without TSC/ECL timing signals. Possible situations for no TSC timing signal are:

- All neutral events
- No charged particle in the acceptance of TSC
- TSC missed charged particle(s) due to its inefficiency
- Something is wrong in TSC trigger system.

Possible situations for even no ECL timing signal are:

- Bhabha process, which has hits only on EFC
- No particle in the acceptance of ECL (particles might pass through the gap of ECL)
- ECL missed particle(s) due to its inefficiency
- Something is wrong in ECL trigger system.

The cue signal arrives after passing through FTDL and PSNM, so it will be late by four 32MHz clocks. If two PSNM's are cascaded, it will be late by six 32MHz clocks. Oppositely, scince there are some loose condition channels at FTDL, the cue signal which is the OR of these FTDL outputs sometimes come earlier than the timing signals. So TMDL should wait for some time before asserting the final trigger of type 2, to make sure that there's really no timing signal. The time to wait is currently set to $t_{wait}^{type2} = 500$ ns, considering the jitter of those loose condition trigger at FTDL comes from the fluctuation of CDC trigger which is around 500 ns, The requirements to this cue signal is, roughly speaking[1],

- Should not arrive at TMDL earlier than the latest ECL timing signal by 500 ns or more, otherwise TMDL will assert final trigger with type 2 and cannot assert with type 1 for the late ECL timing signal.

[1]Exactly speaking, some processing margin should be taken into account.

- Should not arrive at TMDL later than the earliest ECL timing signal by 350 ns or more, otherwise TMDL cannot assert final trigger with type 1 for the early ECL timing signal.

Supposing the ECL timing comes at around t = 1850 ± 100 ns, this condition is read as,

1. The cue signal should not arrive at TMDL before t = 1.45 μs
2. The cue signal should arrive before t = 2.1 μs.

Since the latest subtriggers should be valid at t = 1.85 μs, adding the processing time of FTDL and PSNM (4 or 6 $\times$ T_{clk}^{FTDL}) to it, it is certain that the cue signal will arrive at TMDL at least until t = 2.038 μs. So the second condition is always satisfied. The first condition is satisfied if the fluctuation of CDC trigger is within 500 ns. Note that this is just a rough estimation and according to the actual timing fluctuations of ECL and CDC subtriggers, the time t_{wait}^{type2} will be set properly.

Estimated as above, the arrival time region allowed for the cue signal is so wide that the flow of "subtrigger-FTDL-PSNM" and "timing signal-TMDL-final trigger" can be treated asynchronously. Just an event drive type asynchronous system design will work.

logic The timing signals are fed into shift registers; TSC into 22 steps shiftregister with 64 MHz clock, ECL into 11 steps with 32 MHz clock, to cover 350 ns time window. The first step of shift register shows the current state (high or low) of the input signal, and the last step shows that of 350 ns ago. The turning point of state low to state high means the arrival of the input signal (leading edge of the input signal), which is interpreted as t = 1.85 μs. So, the moment that the turning point propagated and reached to the last step of the sift register is the time to assert the final trigger (t = 1.85 + 0.35 μs = 2.2 μs)[2].

The system clock planned is external 64MHz ECL clock. 32MHz and 16MHz clocks is made internally from 64MHz clock.

The processing inside TMDL is done by a state machine. Figure 6.4 shows the state diagram.

[2]To reduce the logic resource of the chip, the actual logic implemented is different but equivalent, i.e. first, the turning point of signal is detected, and it is fed into the sift registers. See, the appendix B.0.3.

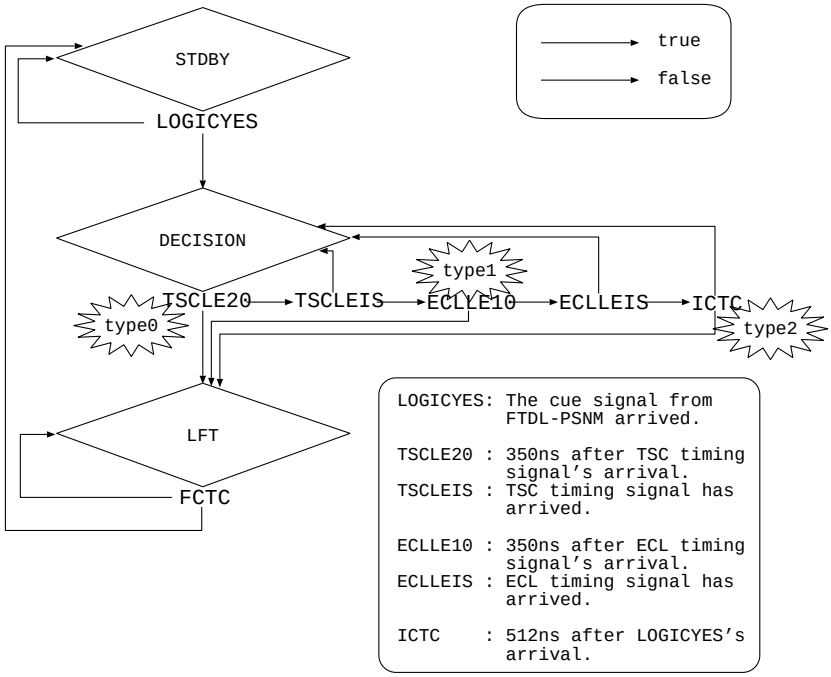

Figure 6.4: State Diagram of Timing Decision

There are 3 states which can be switched with 64 MHz clock. STDBY is the default state to wait for the cue signal. Receiving the cue signal, it moves to DECISION state to decide the final trigger timing according to the following loop. Note that an internal timer which counts till 500 ns is started when moved into DECISION state.

1. Check if the leading edge of TSC timing signal reached to the last step of the shift register. If it is true, assert the final trigger with the trigger type 0, and move to LFT state.

2. Else, check if the leading edge of TSC timing signal has come to TMDL and propergating at some former step of the shift register. If true, go back to DECISION state, stopping the internal timer.

3. Else, check if the leading edge of ECL timing signal reached to the last step of the shift register. If true, assert the final trigger with the trigger type 1, and move to LFT state.

4. Else, check if the leading edge of ECL timing signal has come to TMDL and propergating at some former step of the shift register. If true, go back to DECISION state, stopping the internal timer.

5. Else, check if the internal timer has counted 500 ns. If true, assert the final trigger with trigger type 2, and move to LFT state.

6. Else, go back to DECISION state, *without* stopping the internal timer.

Going on this loop, eventually it asserts the final trigger and comes to LFT state. In LFT, the final trigger is kept active for at least two 16 MHz clocks, and it stays there for two more 16 MHz clocks to block the next trigger[3], and after that go back to STDBY state. This is the one trigger cycle. In the actual design, time out function is equipped to break an unexpected infinite loop at any state other than STDBY, which will logically never happen.

hardware The TMDL module is designed, manufactured, and checked its performance (7.4). Its specification and feature is summarized as follows.

- Single width 6U VME module

[3]This is the requirement from the sequence controller.

- Total 64 TTL I/Os which are received/transmitted through normal pitch 17 pair flat cable connectors at the front panel. 12 of them are connected to PSNM. 5 of them are to put out TTL final trigger and TTL trigger type.
- 8 ECL inputs and 8 ECL outputs which are receive/transmitted through normal pitch 8 pair flat cable connectors at the front pannel. 2 of the inputs are for the timing signal from TSC and ECL. 5 of the outputs are for ECL final trigger and ECL trigger type which is given to the sequence controller.
- Two Xilinx CPLDs (XC95108-7PQ160)
- Timing Decision Logic is downloadable via VME bus
- Two NIM inputs through a double lemo connector for system clock
- One ECL input through a lemo-0 connector for system clock
- Works with 64 MHz clock
- Consumes at least 1 clock to assert the final trigger (in order to move to DECISION state)
- Only one board is used in GDL

See the appendix B.0.3 for more details.

6.3.4 ITD

As is mentioned in 6.3.1, the input signals to FTDL should be adjusted to cover t = 1.85 μs. Also as mentioned in 6.3.3, the timing signal inputs to TMDL should be adjusted their leading edge to come at t = 1.85 μs on avarage. This ITD (Input Trigger Delay) module latches the input signals by the system clock (32 MHz for FTDL, 64 MHz for TMDL) and makes delays to adjust the timing of each signal. The delay value can be set in the unit of the system clock for each input channel via VME bus.

logic The way to make programmable delay is to let the signal pass through a proper number of shift registers. One can set a value of delay in a register, and according to the value, the gate choses the path of signal through the shift register or bypass. See figure 6.5.

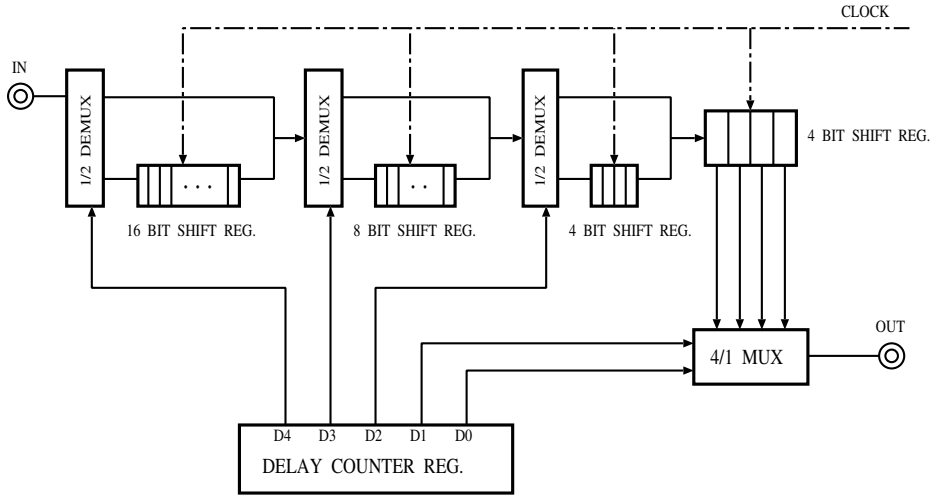

Figure 6.5: Input Trigger Delay Logic

hardware This module is developed and manufactured in USTC, China. Specification is,

- Single width 6U VME module
- 16 ECL inputs through a normal pitch 17 pairs flat cable connector at the front panel
- 16 ECL and 16 TTL outputs through normal pitch 17 pairs flat cable connectors at the front panel
- 5 Xilinx FPGAs (XC3130 for logic part)
- Delay value is loadable via VME bus

- One NIM and one ECL external clock input; NIM is received by a lemo connector and ECL by a normal pitch twist pair cable connector
- Range of delay : 0 to 31 in unit of external clock
- Works with 64 MHz clock

Refer to *ref.*[14] for more detail.

6.3.5 Fan out

Since the GDL input signal travels a long distance from each detector subtrigger system, we use differential ECL signals. And the fastbus TDC which is the standard DAQ readout module accepts ECL inputs. On the other hand, Xilinx CPLD is TTL compatible CMOS chip. Therefore the signals should be converted ECL to TTL and TTL to ECL, according to input/output levels of modules. Additionally, in order to monitor or acquire the informations of GDL, we must fan out the data flow. This module is designed to perform both of these two functions.

This module can treat either TTL or ECL inputs by re-mounting chips on the board, so *not* simultaneously.

Below is the specification.

- Single Width 6U VME module
- No VME access, just taking power from VME crate.
- Allows 16 TTL (ECL) input received by a normal pitch 17 pairs flat cable connector and drives 32 TTL and 32 ECL outputs also through normal pitch 17 pairs flat cable connectors.
- Module propergation delay $\sim$ 16ns
- Total 14 boards are used in GDL.

See, appendix B.0.4 for more details.

6.3.6 Readout Buffers

We must have a DAQ readout buffer module to record the event-trigger information. The following information are stored in the buffer and readout by the DAQ system (event builder).

- Input subtriggers (ITD inputs)
- Timing adjusted input subtriggers (ITD outputs / FTDL inputs)
- Triggerd event type informations (FTDL outputs / PNSM inputs)
- Prescaled event type informations (PSNM outputs)
- Final trigger timing and type information (TMDL outputs)

There're two candidate for this interface module; TDC and TIMS. We'll use either or both of them.

TDC

TDC (Time to Digital Converter) is, as mentioned in chapter 5, the standard interface of the event builder and the detector. We use LeCroy MODEL 1877S 96 channel FASTBUS TDC.

TDC also helps to measure the module performance, such as jitter, delay, maximum clock rate, and so on, which is written in chapter 7.

The specification[11] is,

- Single width FASTBUS module
- 96 channels per module
- 500 ps resolution (LSB)
- Programmable full scale up to 32 μs
- Up to 16 hits/channel (programmable)
- Rising and/or Falling edge timing information
- Multiple event buffer (8 buffers)

TIMS

Actually the specification of LeCroy FASTBUS TDC is excellent as an interface to DAQ, however, it has some problems.

1. It is quite expensive. It costs around 1M yen for one module. Too expensive module might mean no stock when it goes out of order.
2. It requires FASTBUS crate and other interface modules to VME, and experience with FASTBUS.
3. It obtains too much information of inputs and the data size becomes large.
4. It requires analysis to know the input informations.

So we have a plan to develop an interface module between DAQ and GDL, which is called as TIMS (Trigger Information Monitoring System).
The specification of TIMS is,

- Single width VME module
- Shift register + Dual Port Memory
- Time resolution same to the system clock.

This module will solve all of the above problems. In appendix B.0.5, the design of this board is shown.

6.3.7 Scaler

The Readout Buffers are to get the informations of those which are taken as a event. On the other hand, this Scaler is to get the number information of those which are rejected at FTDL or PSNM. The following is the list of the information monitored by this Scaler.

- Number of timing adjusted input subtriggers (ITD outputs / FTDL inputs)
- Number of the event type triggers (FTDL outputs / PSNM inputs)
- Number of prescaled event type triggers (PSNM outputs)

- Number of clock count (further prescaled RF signal)

These're counted with and without BUSY signal of sequence controller in order to know the dead time. These scalers are operated in a latch-and-clear mode and the data are read out in every a few seconds by the sequence control CPU.

HARDWARE This Scaler is implemented on Suehiro module, too. The specification of Scaler is

- 32 16-bit counters per module; half are veto counters and the other half are without veto facility. i.e. 16 channels per module
- Channel by channel clear,
- Channel by channel latch and readout from VME.

It is going to be upgraded to have a latch-and-clear mode:

- Simultaneous clear all channels,
- Simultaneous latch all channels and readout.

See the appendix B.0.7 for more details about current design.

6.3.8 RFCG

As mentioned in section 6.1, we need the RF signal to get the system clock and make the system work. But, until the accelerator is on, we will not get the RF signal. So we need a clock generator instead of it, when there is no accelerator operation. This is not only for GDL system, also all of the subtrigger systems requires this clock generator.

The specification is,

- Single width NIM module.
- 64 MHz, 32 MHz, 16 MHz, and 100 KHz synchronized clock outputs with NIM and ECL.

- NIM is from lemo connectors and ECL is from a normal pitch 5 pair flat cable connector[1].

Note that the duty factor of 100 KHz clock is not 50 %. It's active for the time same to 16 MHz clock period(62.5 ns). See the appendix B.0.6 for more details.

6.3.9 PPG

PPG (Pulse Pattern Generator) is developed by KEK Electronics Facility. We can set an arbitrary 16 bit $\times$ 4K depth pattern in a data RAM, and run it with one depth / one clock sequentially. We can run it continuously and we get 16 ECL periodic outputs per one module. This is quite useful as a test input pattern generator to each function modules of GDL. For GDL, we run three PPGs synchronously to obtain 48 channels of test pattern.

[1]There is a version up plan to lemo-0 connectors.

Chapter 7

Performance Measurement

Entire GDL scheme and modules have been designed as described in chapter 6. All GDL modules except TIMS are made or obtained in some way, so far.

The performance of these modules must be checked carefully; first each module should be checked independently, next combined with the neighboring module, next as a whole GDL trigger system, and finally together with subtrigger systems; before the beam commissioning in October 1998.

In this chapter the individual performances of ITD, FTDL, PSNM and TMDL are reported. The check points are these two.

- The maximum clock frequency with which the system can work properly as a pipeline.
- The minimum input pulse width which can be latched safely with the system clock.

The basic setup is shown in figure 7.1 for FTDL case as an example. Principle of measurement is as follows.

1. PPG generates a periodic test pattern (ECL) with some changeable width. It can be both synchronous/asynchronous to the system clock. Basically it is done asynchronously.
2. It is fanned out by F/O(1,2), and TTL outputs are given to the sample (FTDL in figure 7.1 case) and ECL outputs are given as the TDC input signals.

3. In the sample, it goes with changeable system clock.

4. Outputs from the sample are converted from TTL to ECL by F/O(3) and given also to the TDC as start signals.

5. PPG also generates a trigger signal once in a period, and it is given to a gate generator.

6. The gate generator delays the trigger signal for some amount ($\sim$150 ns[1]) and give same two outputs; one is given to the CAT module to stop (common stop) the TDC, the other is given to another gate generator and further delayed ($\sim$ 96 μs) in order to make time for the TDC to digitize, and finally it is fed into a interrupt register.

7. The interrupt register is just used as an input register here, and the CPU checks this trigger input by polling.

8. After the CPU found this input, it starts data transfer from TDC via dual port memory.

9. After finishing the data transfer, CPU clears TDC by writting value to the interrupt register, which is used as an output register in this case, and wait for the next trigger.

In order to examine whether the module works properly as a pipeline mode, the distribution of the time between the output to input pulses (latency) are checked. The measured distributions are shown by the scatter plot with the system clock period as illustrated in figure 7.2.

In figure 7.2, *the allowed region* means possible input to output time region when the system is working synchronously with the system clock. The line of the smallest delay limit is represented as $y_1 = (n-1)x + offset$, where n is the number of latches between input and output, offset is the residual delay after subtracting output from input, namely the sum of the cable delays of F/O(1,2) to sample, sample to F/O(3), plus the propagation delay in the F/O(3)[2], plus connector to the first flip-flop path delay and the last flip-flop to connector path delay in the sample. This is because the smallest delay will occur when the input signal arrives at the first flip-flop simultaneously with

[1]To increase this delay and to increase the time between the test pattern and the trigger at PPG is equivalent.

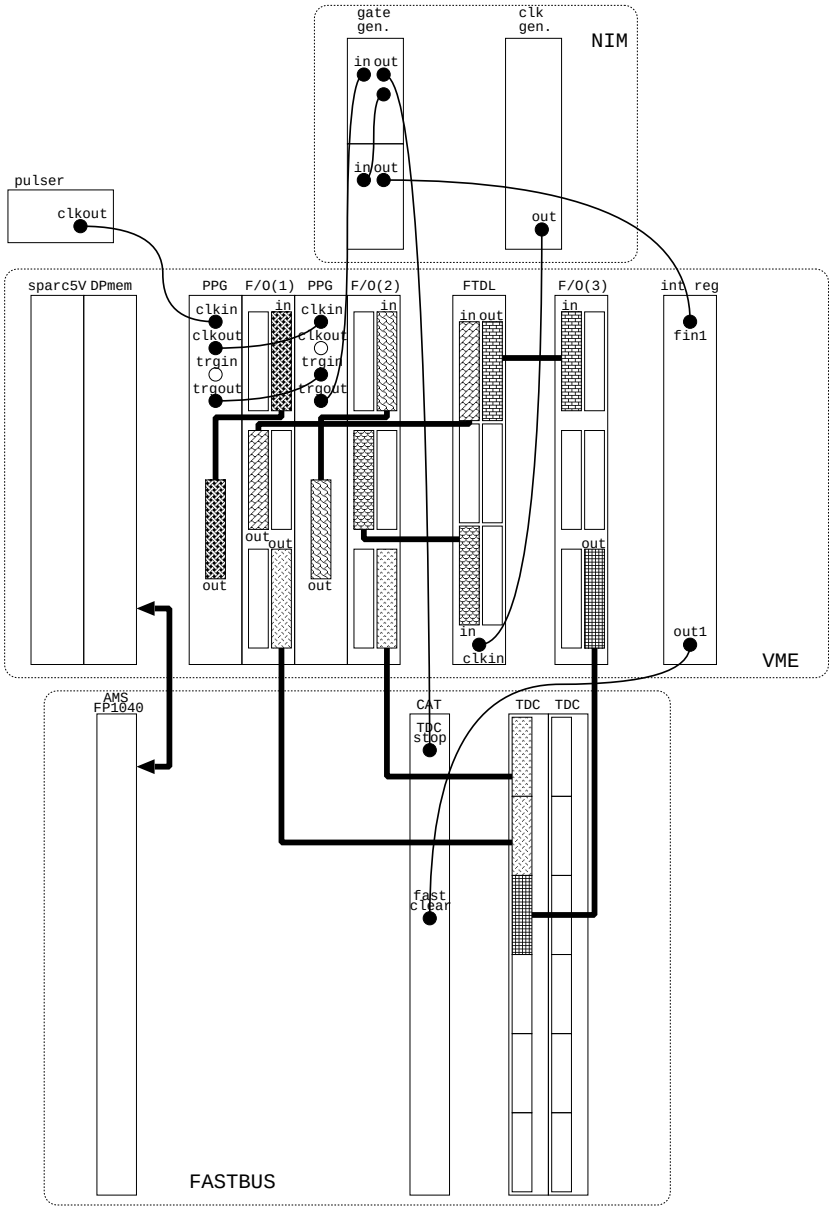

Figure 7.1: Measurement Setup for FTDL

the system clock. In this case, this data will be latched by the second flip-flop with the next clock (one clock period after the signal arrival). Going on this way, the data is latched by the n-th flip-flop $(n-1)$ clocks after the signal arrival. Figure 7.3 shows y_1 and the measurement offset in the case of FTDL. The line of the largest delay limit is represented as $y_2 = nx + offset$, because it will happen when the input signal arrives at the first flip-flop right after the system clock. Thus, the possible distribution width $y_3 = y_2 - y_1 = x$ is proportional to the system clock period. It can be deduced that so long as the input to output latency distribution is inside *the allowed region*, the system is working properly with that period of system clock. It is easily expected that with rather short period clock, i.e with rather high frequency clock, the distribution of the latency go out of bounds of the *allowed region* to the upper region of y_2. In the following sections, The graph of "the latency vs the system clock period" is shown in order to see the maximum system clock frequency, and say the safeness to run with the clock frequency planned.

The other check point, the minimum input pulse width to be latched safely is measured with fixed system clock frequency which is planned to use actually, changing the input pulse width gradually, instead. If the number of outputs is less than the number of inputs, it is due to the latch inefficiency at the sample, supposing there is no other inefficiency in the system, for example at TDC. First, the inefficiency of the system is concluded to be less than 10^{-6} (CL 95%), because there was no missing pulse in more than 3M events[3].

Generally, it is expected that the latch efficiency for the input pulse whose width is shorter than the system clock period is the ratio of input pulse width and the system clock period, i.e.

$$R_{latch} = \frac{T_{input}}{T_{clock}}.$$

So, the mis-latch ratio is

$$R_{mislatch} = 1 - \frac{T_{input}}{T_{clock}},$$

[2]The sum of the cable delay and F/O(3) propergation delay is measured and that was around 28ns.

[3]While using a single twist pair cable, about 100 events / 500K events were lost, due to the rickety connector.

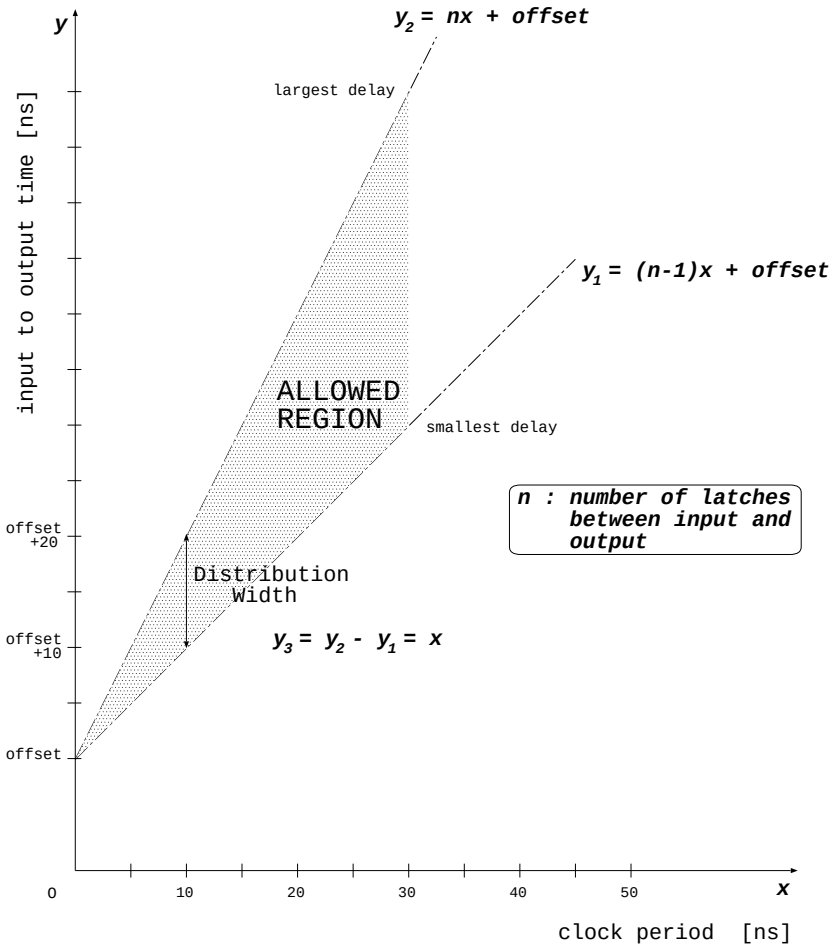

Figure 7.2: Input to Output Delay Time Allowed Region

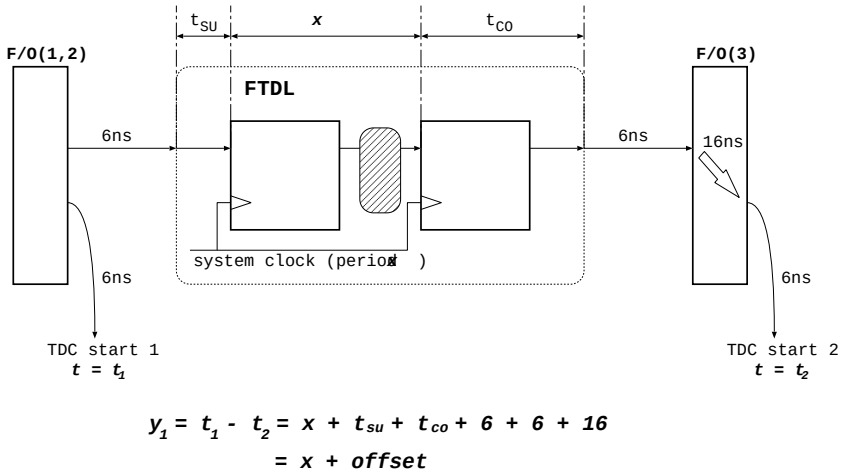

Figure 7.3: Measurement Offset and the smallest latency of FTDL

and

$$\frac{dR_{mislatch}}{dT_{input}} = -\frac{1}{T_{clock}}. \tag{7.1}$$

Note that T_{margin} which is mentioned in 6.3.1 is determined from the consequence of this measurement.

7.1 FTDL

Maximum Clock Rate In the current design of FTDL shown as an example in table 6.1, there are 26 inputs and 15 outputs. 21 typical input patterns out of 2^{25} possible combinations are fed in and checked. These are listed in table B.2. Basic manner to check and/or gates is change only one input while others are kept constant.

First the output pattern is checked and no artificial error in logic was found. Next, input to output delay is measured with system clock frequency, 25, 32, 40, 55, 80, 85, 90, 95, 100 MHz for each 21 patterns; 10K events for each input pattern. The width of input signal is chosen as 50ns so that it can be latched safely by even 25MHz clock.

Figures 7.4, 7.5, 7.6 are the 2D and 3D plot of latency distribution for both leading and trailing edge. Here, leading edge is rising edge for nomal inputs and falling edge for veto inputs (ECL:BB and ECL:cosmic); trailing edge is vice versa. In the figure, all the case of 21 input patterns to corresponding outputs are superimposed, so each pile contains 430K events. Note that the resolution of TDC is 0.5 ns.

In these figures, we can see the latency distribution is inside *the allowed region* for the system clock period larger than 12.5 ns, ignoring the tiny seepage from the boundary due to the jitter of measurement. The mis-pipe ratio, or "not allowed" ratio, is as follows. Mispipe ratio at 80 MHz is

Table 7.1: FTDL mispipe ratio

clock [MHz]	leading edge	trailing edge
100	33%	96%
95	15%	60%
90	8%	30%
85	0.8%	0.5%
80	$\leq$0.03%	$\leq$0.03%

estimated as less than 3×10^{-4} (95 % CL), for each channel[1]. We're going to operate with 32MHz clock and it can be concluded that FTDL can work with 32MHz clock quite safely.

Minimum Input Pulse Width Efficiency to latch the input pulse is measured with external 32MHz clock. In the current design, FTDL has 25 input flip-flops and they are destributed in 6 function blocks (FB). Input no. 0 and 15 (see, table 6.1) which belong to FB5 and FB3, respectively, are checked as representatives.

Figure 7.7 shows the ratio of mis-latch vs the input pulse width. The input pulse width is actually measured by TDC, at the same time. It shows that the slope of the measured data is -1/31.25 and consistent with the expectation of the equation 7.1. In order to latch the input signal safely, the

[1]According to the timing simulator (one of the development tool), it is guaranteed to work only upto 55MHz clock.

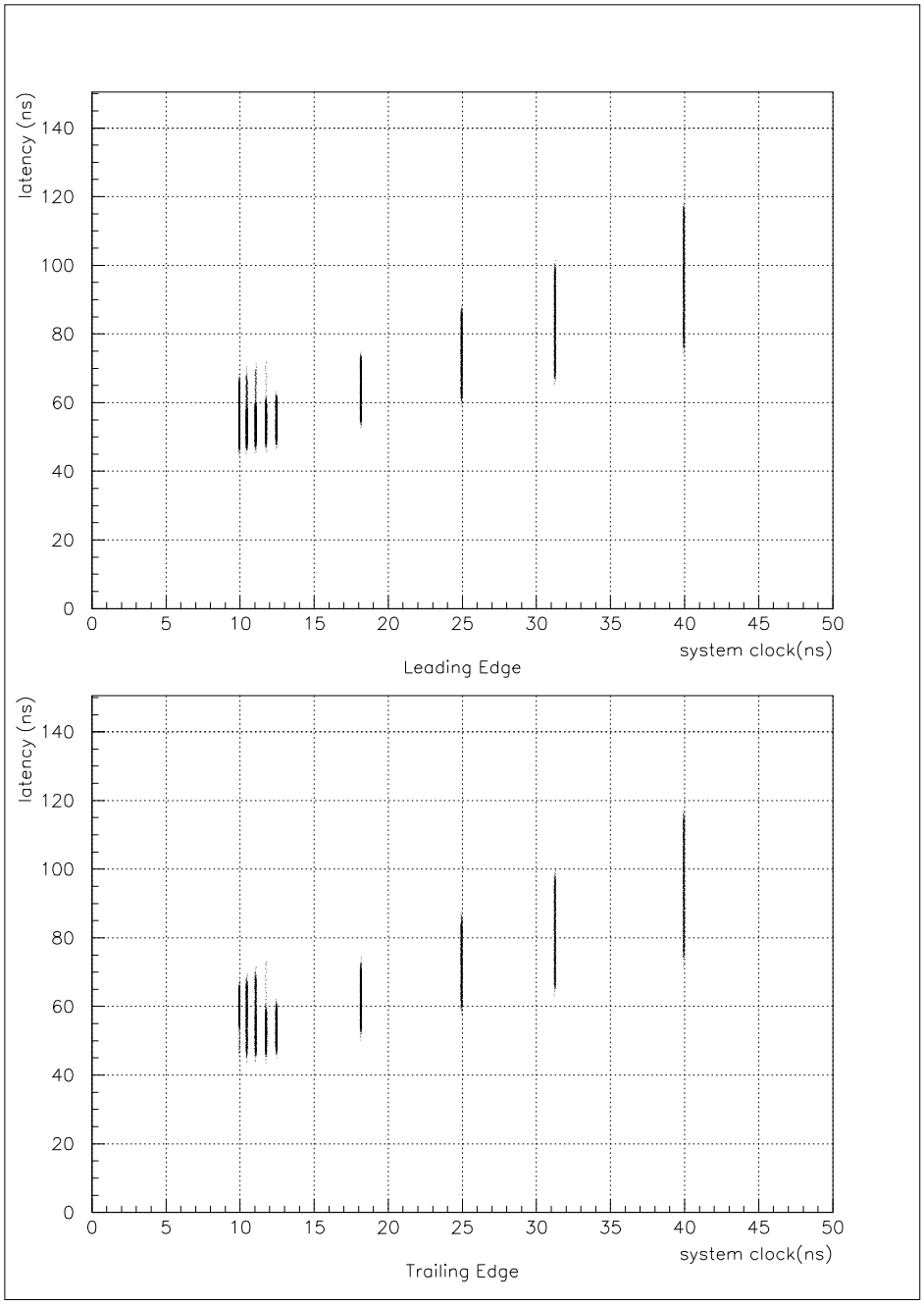

Figure 7.4: Input to Output Latency vs System Clock Period

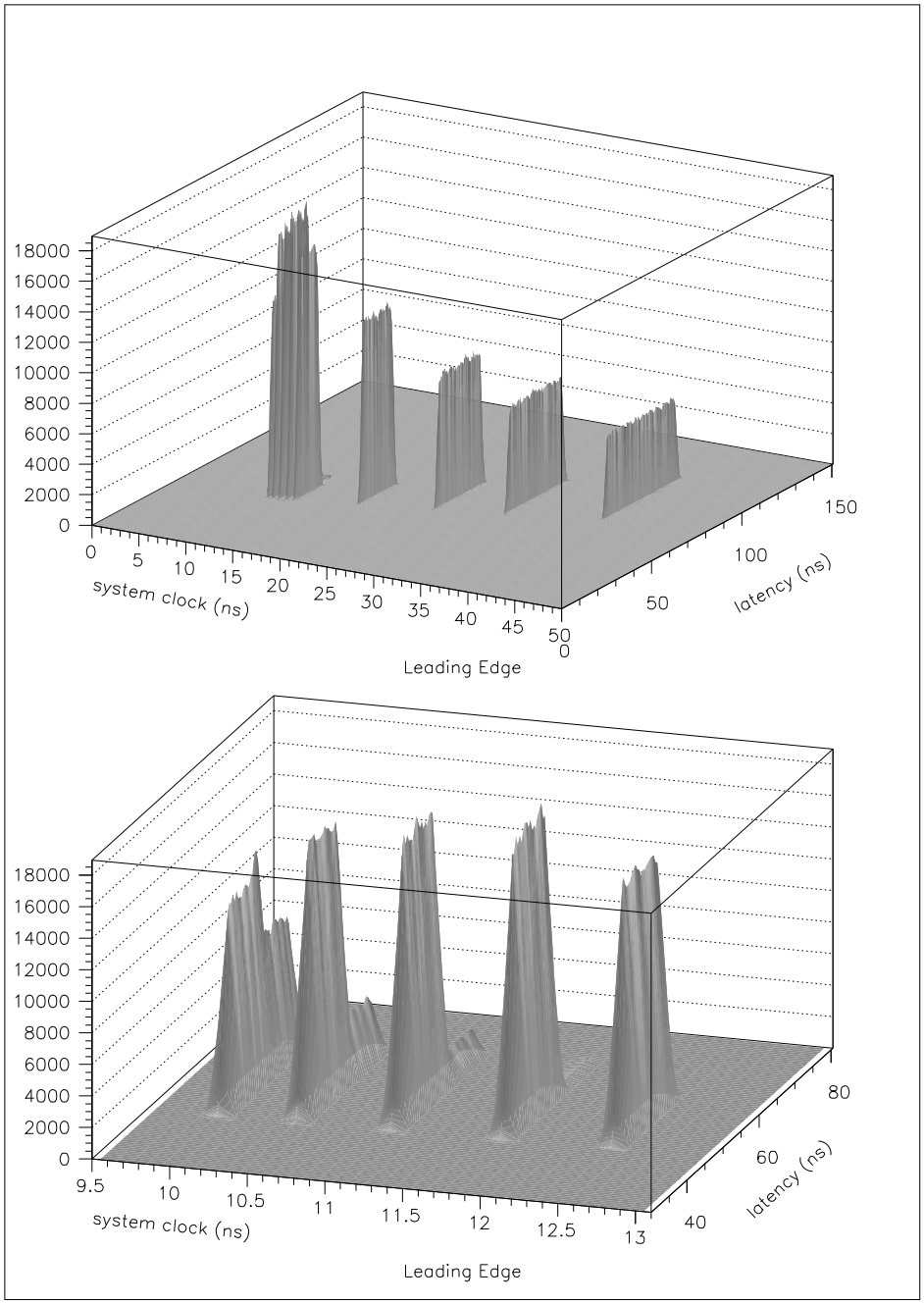

Figure 7.5: Input to Output Latency vs System Clock Period (leading edge)

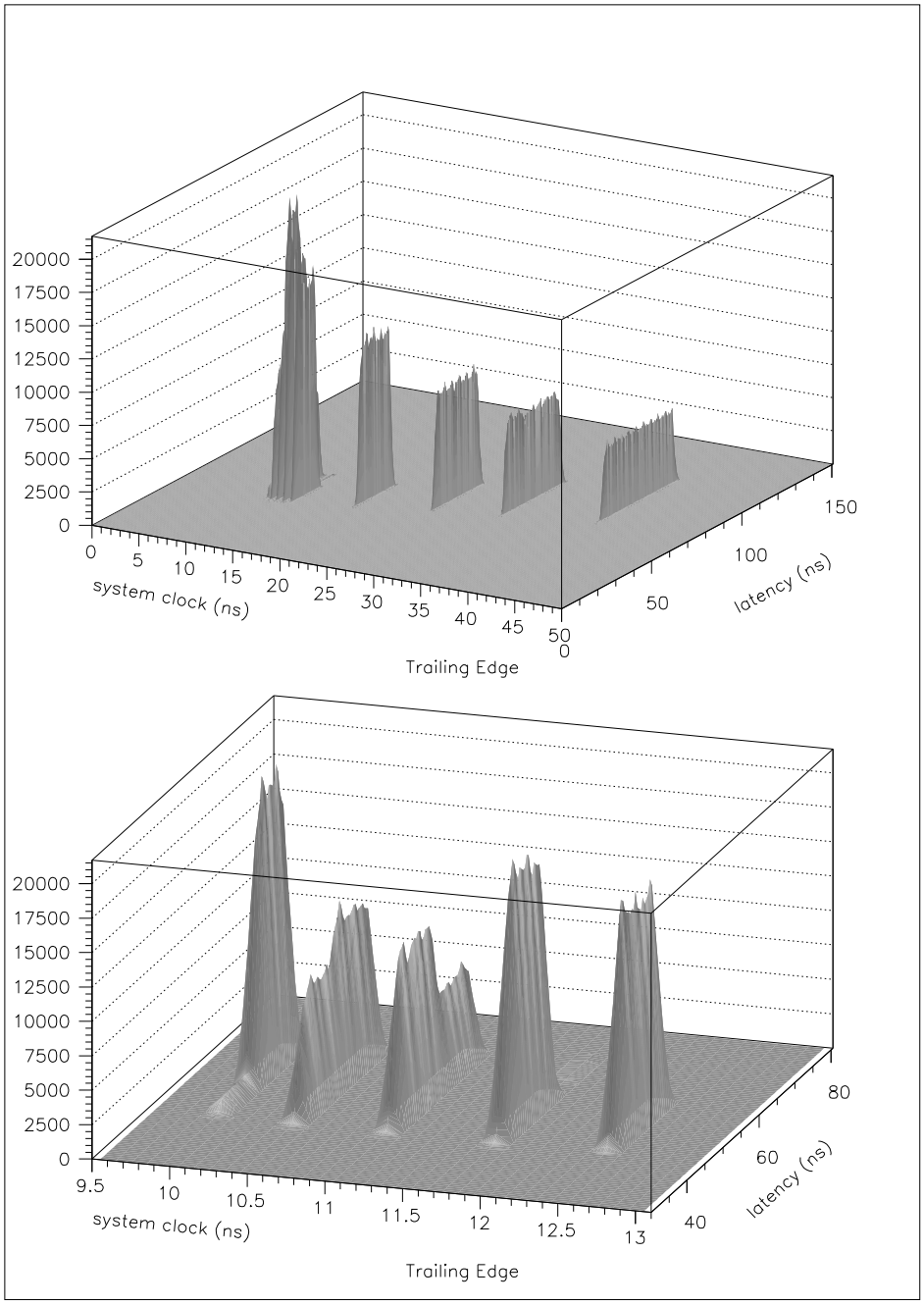

Figure 7.6: Input to Output vs System Clock Period (trailing edge)

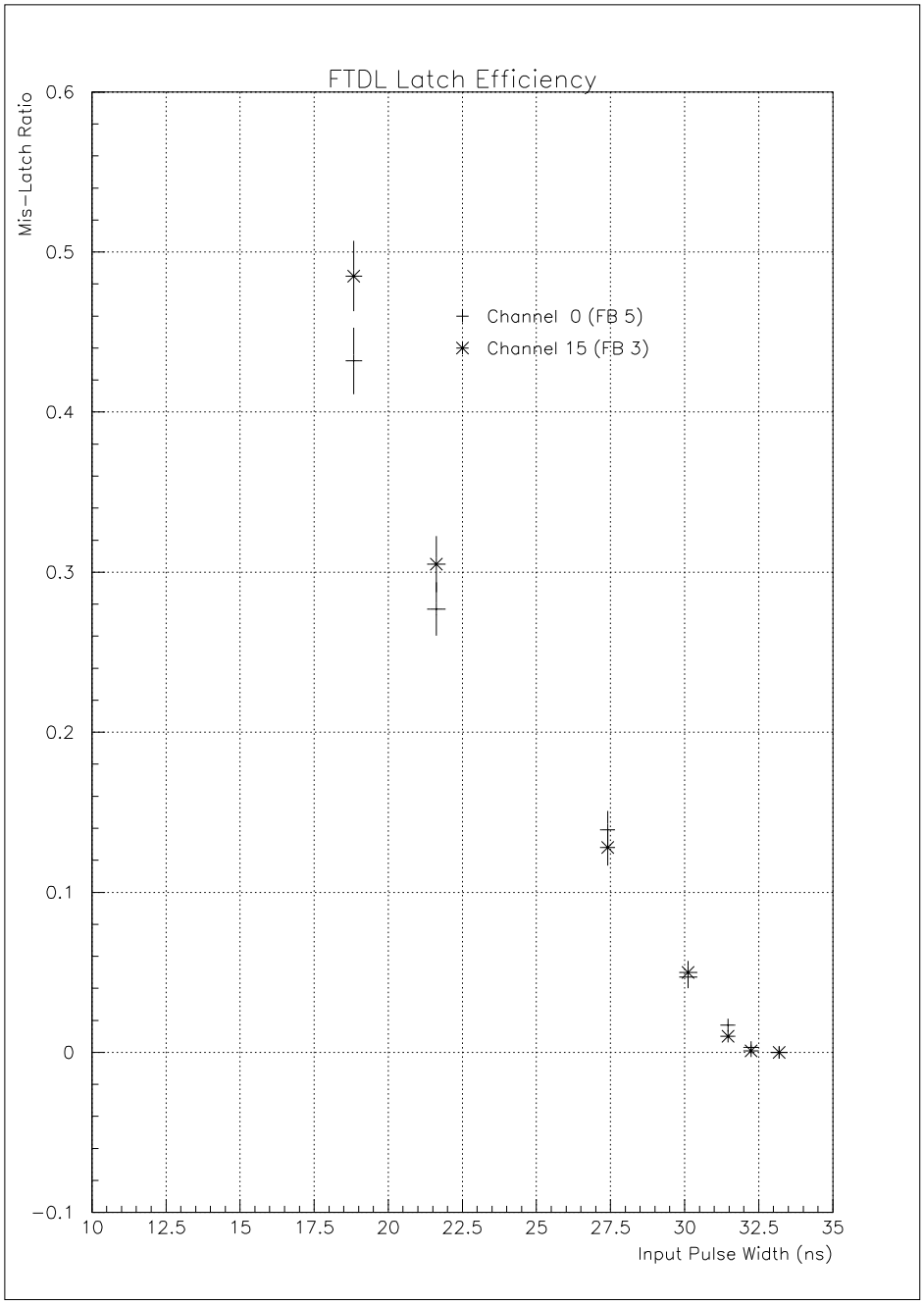

Figure 7.7: Mislatch ratio of FTDL at 32MHz operation

width should be greater than 33.5ns (probability of failure : 3×10^{-5} CL 95%).

7.2 ITD

Maximum Clock Rate ITD has 16 channels per board and each channel can accept 0 to 31 as the delay value. Changing the delay value means the change of signal path and the number of flip-flops between input and output. So, the max clock rate measurement is done for each delay value. Measurement points are chosen at 25, 32, 45, 64, 70, 85 MHz, and more than 2500 events are taken for each point. External ECL clock is used and NIM clock is not used here. The width of input signals is also chosen as 50ns.

Figures 7.8 to 7.15 show the input to output latency vs system clock period for both leading and trailing edges of TTL and ECL outputs. The even and odd delay values are ploted in different figure. (See the caption of each figure.)

Mispipe is not seen in all of these plots, and the mispipe ratio at 85MHz is estimated as as less than 1.2×10^{-3} (95 % CL). We're going to operate ITD with 64MHz at most, and it can be concluded that ITD can work with 64MHz clock safely.

Minimum Input Pulse Width Efficiency to latch the input pulse is measured with external 32MHz ECL clock. ITD is also planned to be used with 64MHz clock for TSC and ECL timing signals, yet since they are also fed into FTDL, their width will satisfy the condition for the signal latched by 32MHz clock. So, latching them with 64MHz clock is easier than with 32MHz clock and measuring the latch efficiency with 32MHz clock is enough.

Measurement is done with the delay value shown in table 7.2. These values are chosen, because *the first* flip-flop is different for these delay value.

Figure 7.16 shows the ratio of mis-latch vs the input pulse width. The input pulse width is measured value. It shows that the slope of the measured data is -1/31.25 and consistent with the expectation of the equation 7.1. But there is some 0.05 (5%) offset in the absolute value of mis-latch ratio, which

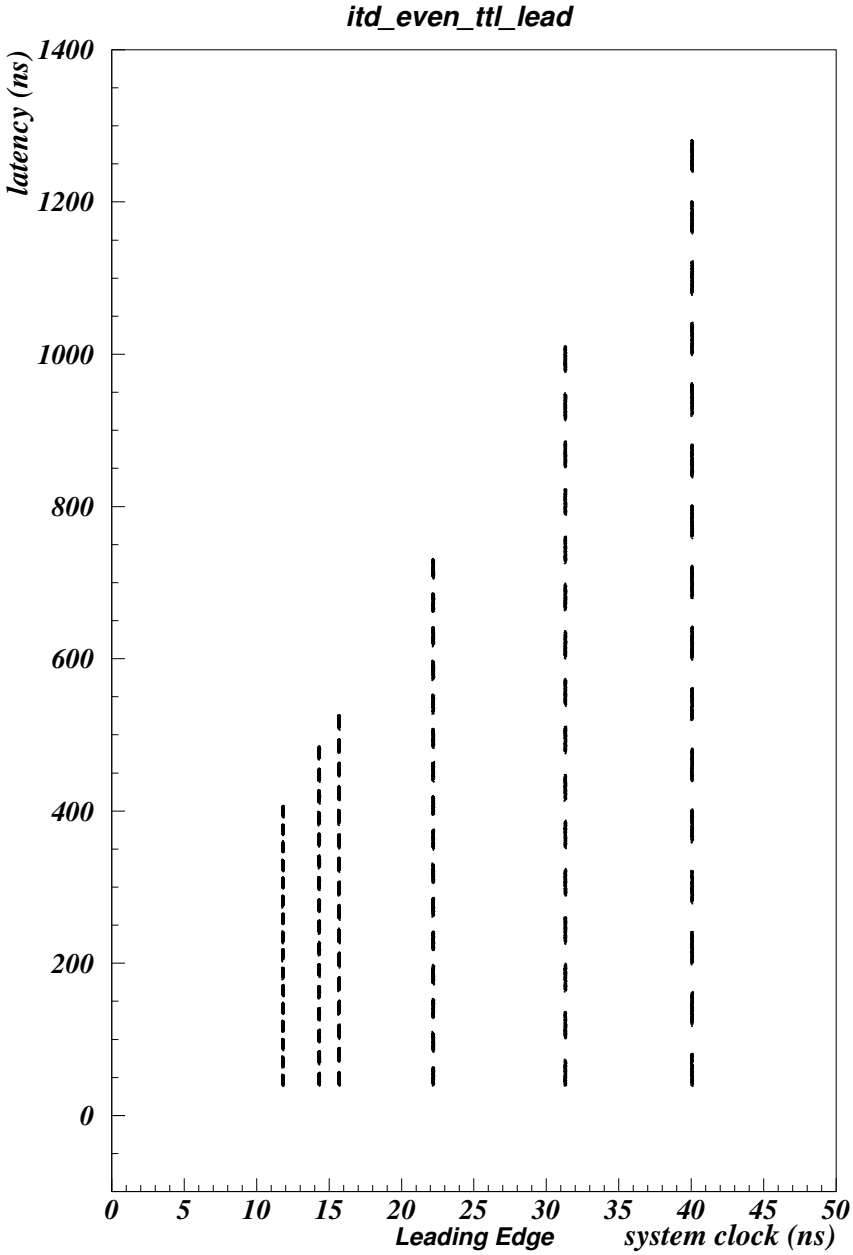

Figure 7.8: The leading edge latency of ITD TTL output for even delay values

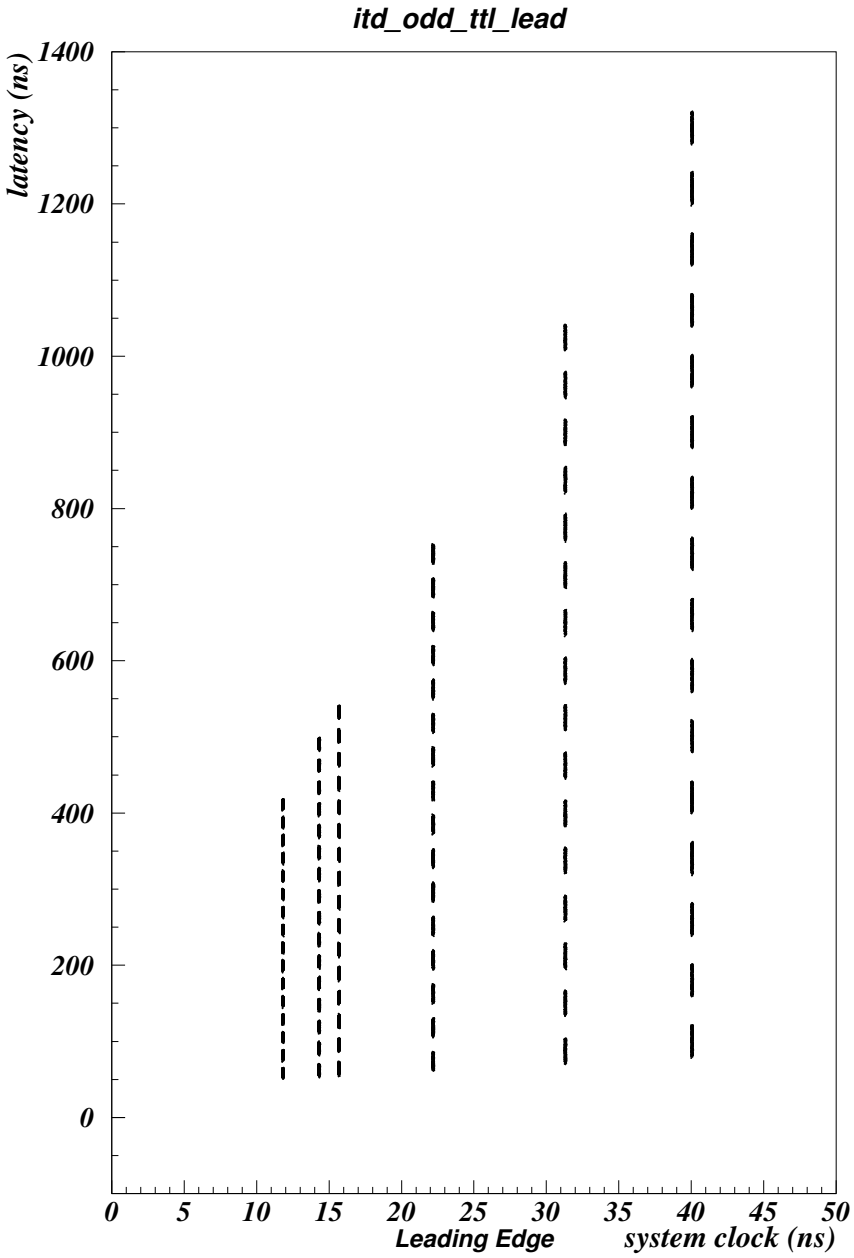

Figure 7.9: The leading edge latency of ITD TTL output for odd delay values

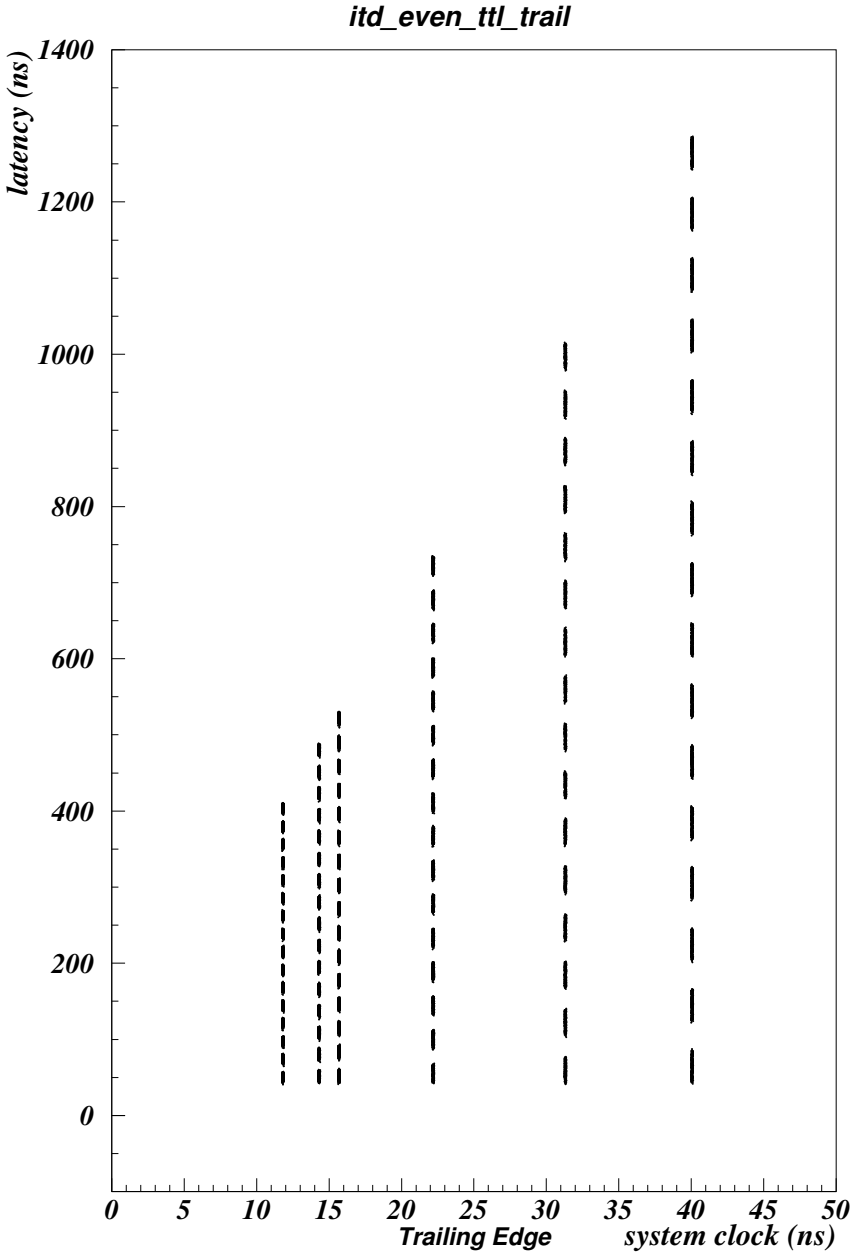

Figure 7.10: The trailing edge latency of ITD TTL output for even delay values

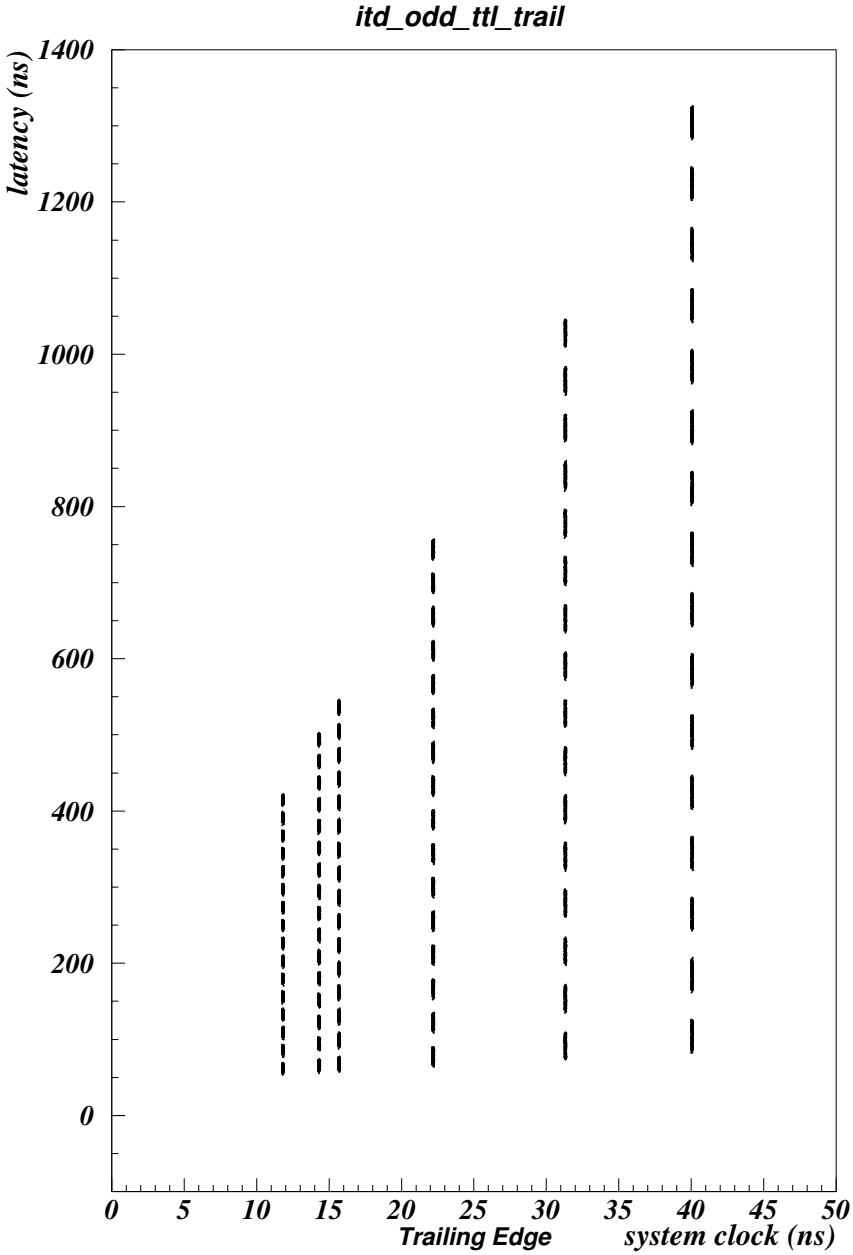

Figure 7.11: The trailing edge latency of ITD TTL output for odd delay values

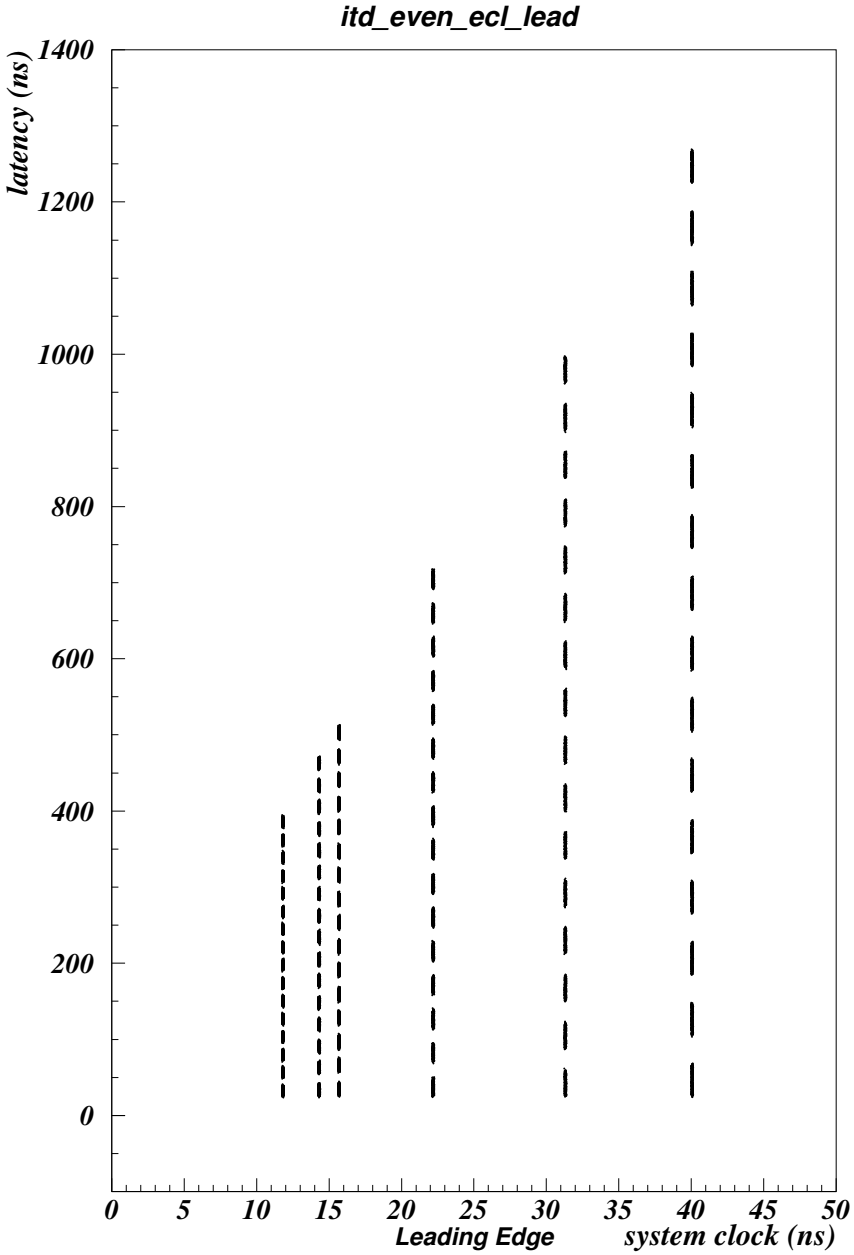

Figure 7.12: The leading edge latency of ITD ECL output for even delay values

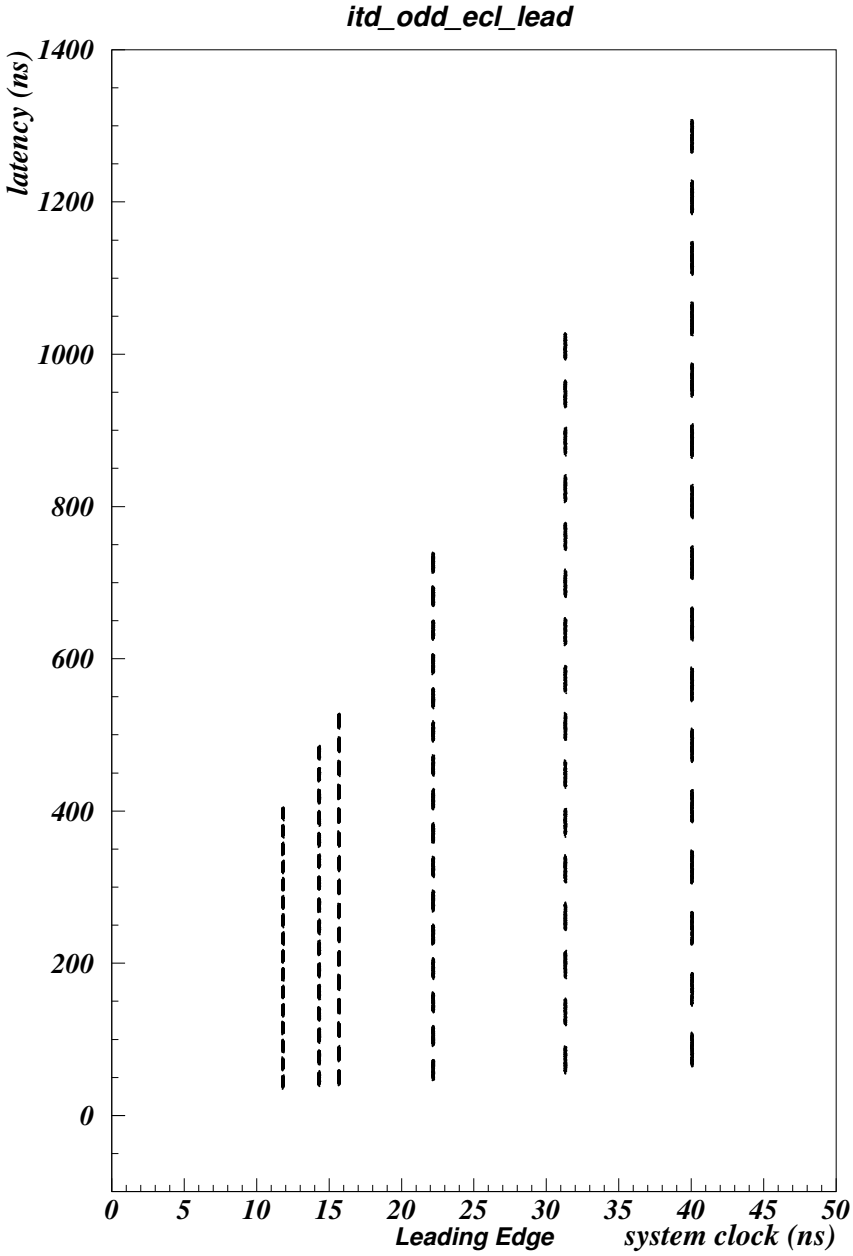

Figure 7.13: The leading edge latency of ITD ECL output for odd delay values

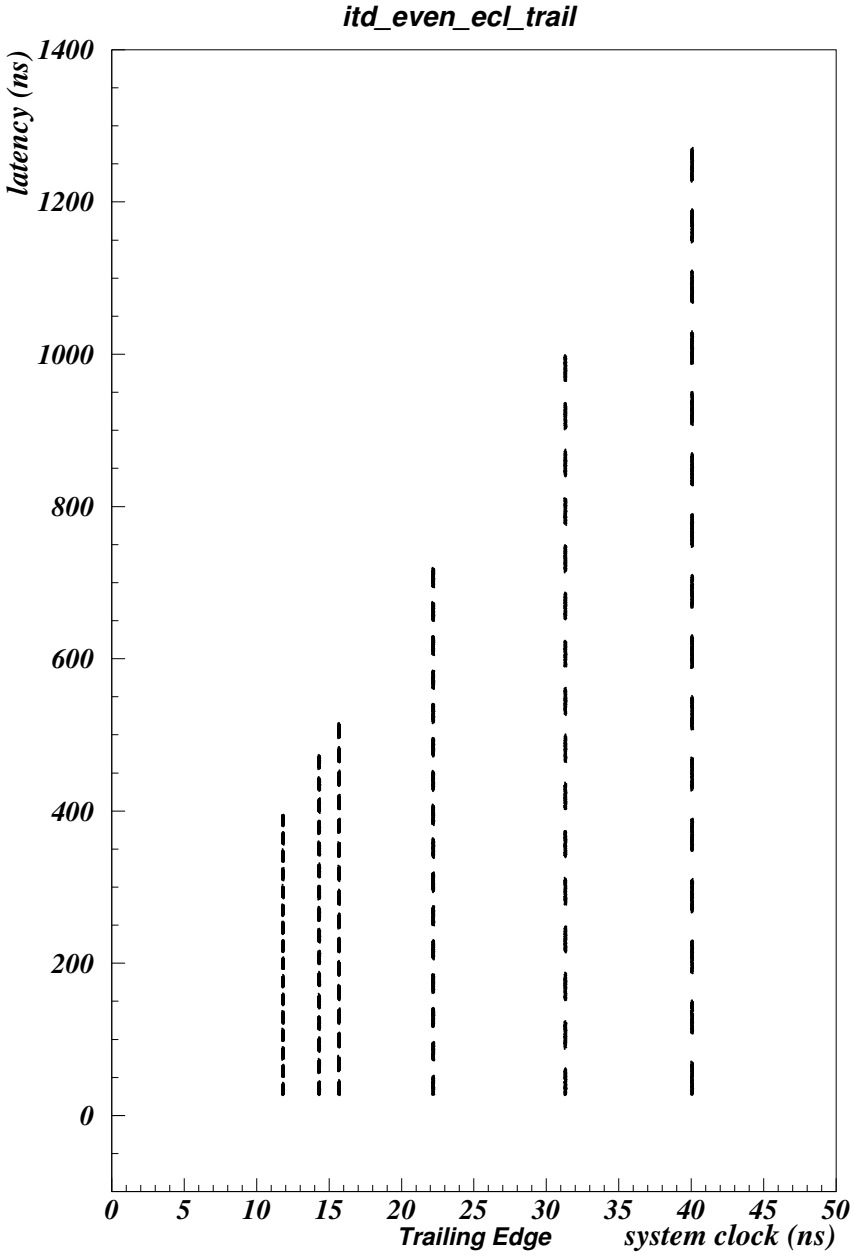

Figure 7.14: The trailing edge latency of ITD ECL output for even delay values

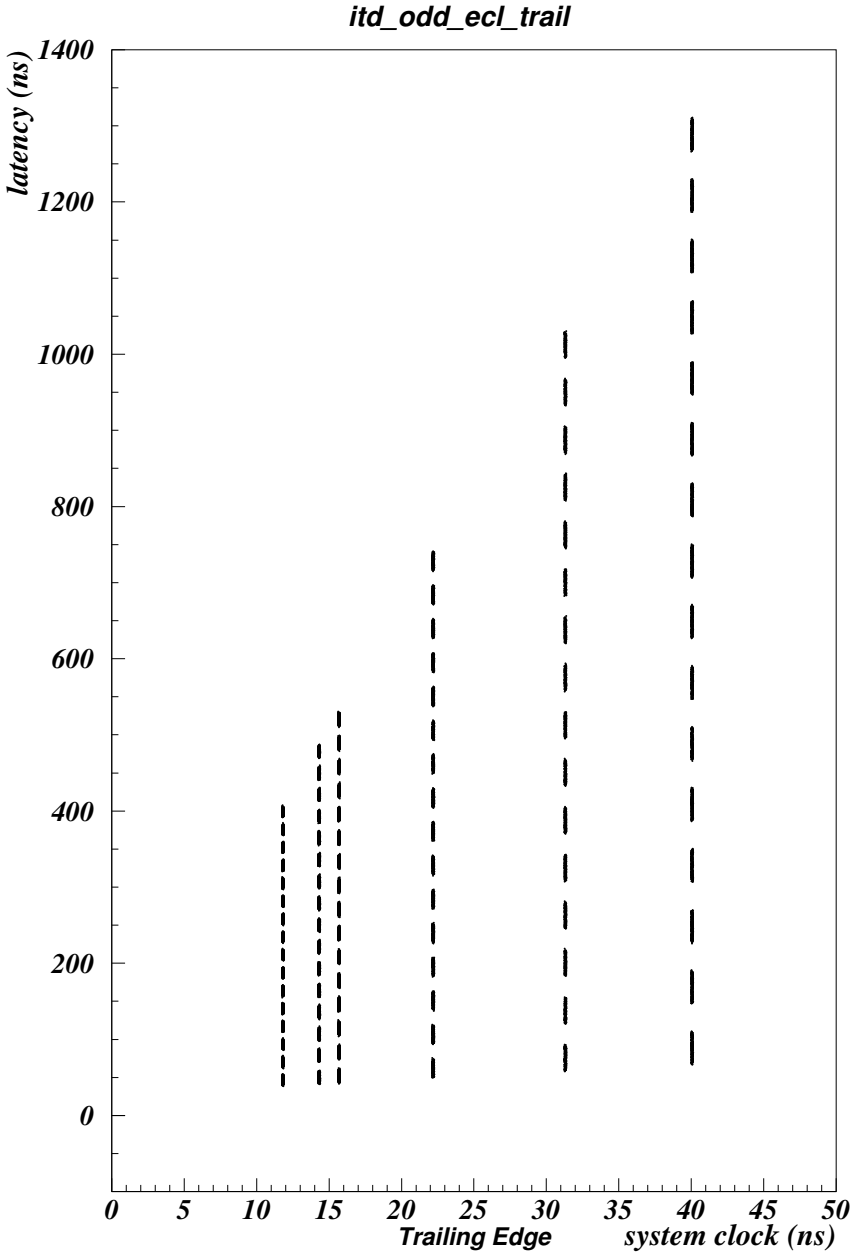

Figure 7.15: The trailing edge latency of ITD ECL output for odd delay values

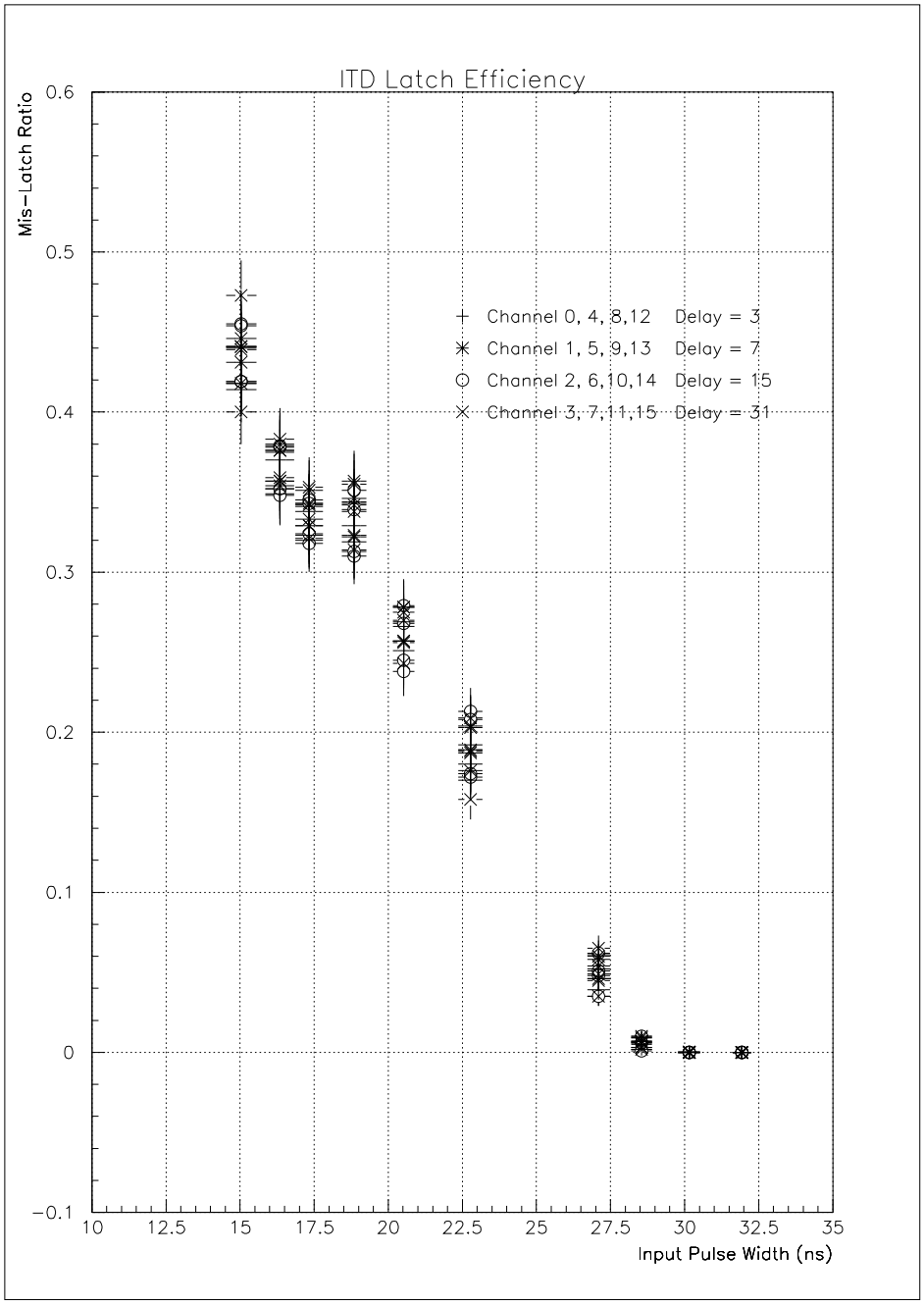

Figure 7.16: Mislatch ratio of ITD at 32MHz operation

Table 7.2: ITD delay set for Latch Efficiency measurement

Delay Value	Channel No.
3	channel0, channel4, channel8, channel12
7	channel1, channel5, channel9, channel13
15	channel2, channel6, channel10,channel14
31	channel3, channel7, channel11,channel15

is not seen in FTDL case. This is because the 10125 chip which is put as the receiver on the ITD board enlarges the signal width by about 2ns[1] while converting from ECL to TTL. Anyway, ITD can latch the input signal safely if its width is greater than 32.2ns (probability of failure $< 2.5 \times 10^{-6}$ CL 95%).

7.3 PSNM

Maximum Clock Rate Among the flip-flops used in PSNM, only two flip-flops per one channel work with the system clock, which latch the input (IFD[1]) and output (OFD[1]). The other flip-flops, which are the components of synchronous counter, are ticked by the latched input signal at IFD. Therefore the severest situation for this system occurs when the frequency of the *input signal* becomes high. However, since the input signal is latched by the system clock, the frequency of input signal cannot go beyond the half of the system clock frequency. So, the measurement is done increasing the frequency of both the system clock and the input signal. The frequency of the input signal is set exactly half of the system clock and the phases of them are locked so that the system clock can latch the input certainly.

The signal path forks at the counter. All the paths from each counter bit through comparator to the D inputs of the terminal count flip-flop should be checked. This can be done by setting different prescale value. However if

[1]Measured for 32ns width input

[1]See, figures B.9 and B.10.

the prescale value is set to 0x81, the D input of the terminal count flip-flop will be 1 when the count become 0x80 from 0x7f, changing the state of all counter bits. In this case, all the signal paths can be checked simultaneously.

The process of measurement is as followings.

1. PPG generates 0x81 pulses with 16MHz frequency. After that it keeps low (0) for about 120μs. Those pulses are fed into TDC start.

2. PSNM prescales by factor 0x81, so only the last pulse goes through. This is also fed into TDC start.

3. PPG generates the trigger signal soon after the 0x81-th pulse and it stops the TDC.

So, checking the time difference of the 0x81-th input pulse and the prescaled pulse, we can see if the PSNM is working properly or not. Figure 7.17 is the latency of the 0x81-th input to the prescaled output vs system clock. Since the input signal is fed into the clock of flip-flop and only the leading edge information is used in PSNM, the plot is only for leading edge latency. 10K events are taken for each system clock, and all channels (0 to 15) of PSNM are superimposed.

In the figure, the distribution width of latency is narrower than the clock period because the input signal and the system clock are synchronous. The latency stays inside the *allowed region* upto 34MHz system clock. The points outside the *allowed region* comes from channel 9 and 11. These two channels are in the same Xilinx chip, and tuning up the signal path of the chip, the performance will be improved. So far, PSNM is operatable upto 34MHz. Error ratio at 34MHz system clock is less than 3×10^{-4} (95% CL).

Minimum Input Pulse Width When the inputs and the system clock are synchronous, no inefficiency was found in 150K events. One event contains 0x81 inputs and none of them are missed. The mislatch ratio is therefore estimated as less than 1.55×10^{-7} (95% CL), for the case the input and the system clock are synchronous.

7.4 TMDL

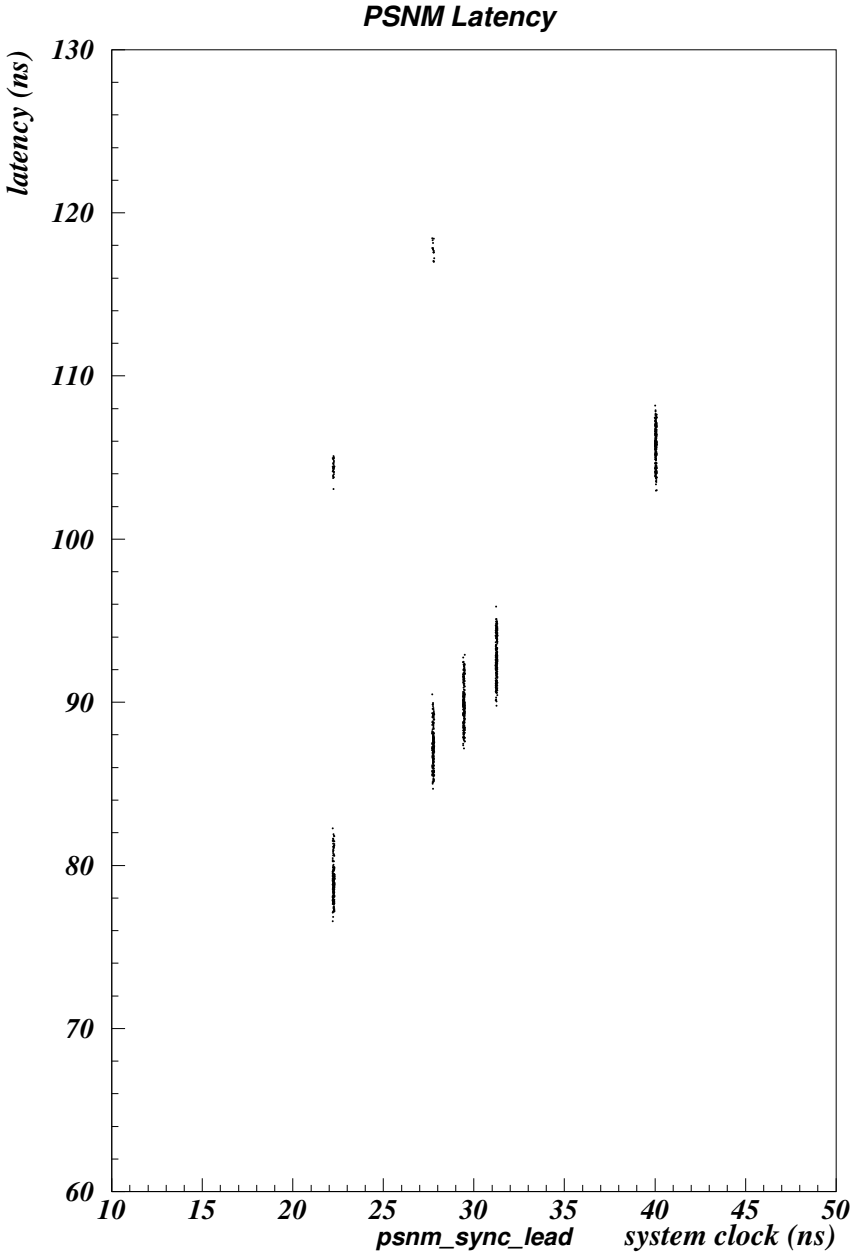

Figure 7.17: Latency between the 0x81-th input and prescaled output by factor 0x81 vs System Clock Period

Maximum Clock Rate In the actual trigger, the TSC, ECL timing signals and the cue signal from PSNM must have some correlation. But here the performance is checked without any correlation between them. The width and frequency of these input signals are set as shown in the table 7.3. The

Table 7.3: TMDL test input signals

Signal Name	Width [ns]	Frequency [KHz]
TSC:timing	46.9	250
ECL:timing	250	312.5
PSNM out	100	10

widths are chosen almost same as the expected actual signal, and the frequency is set much higher than that.

The Xilinx chip planned to use for TMDL is XC95108-7PQ160, yet the system test is done using the same chip but with speed grade -10[1].

The test is done with upto 95MHz clock. For more than 75MHz, the system could not run properly. Since TMDL is a complicated cluster of synchronous flip-flops, the functionality of TMDL changes drastically[2] and it does not behave as expected at all. So, the false behavior of TMDL at high system clock frequency cannot be shown like that of the other modules. Therefore the latency is plotted only for 70, 64, 55, 50, 45 MHz (figure 7.18 to 7.20). 20000 events are taken for each clock; half was trigger type 2, the half of the rest was trigger type 1 and the rest was trigger type 0. No mistake was found in the timing selection logic.

Figure 7.18, 7.19 and 7.20 shows the latency of timing source (TSC, ECL and the cue signal) to the (a)ECL and (b)TTL final trigger. The designed latency is 350ns, 350ns and 500ns at 64MHz system clock, respectively. There are some points in the upper region of *allowed region*. This disallowed ratio is listed in the table 7.4. The ratio does not depend on the clock so much, and

[1]The reason why -10 chip was used is just because there was no available -7 chip with us. According to the timing simulator, the TMDL does not work with 64MHz, using -10 chip, and works using -7 chip. In case of FTDL we saw that it works with 80MHz clock while the timing simulator says the maximum is 55MHz, so this test is not in vain.

[2]The state cannot move to the next state properly, and it lose the consistency, and consequently, for example, multiple final triggers are asserted from one cue signal, etc.

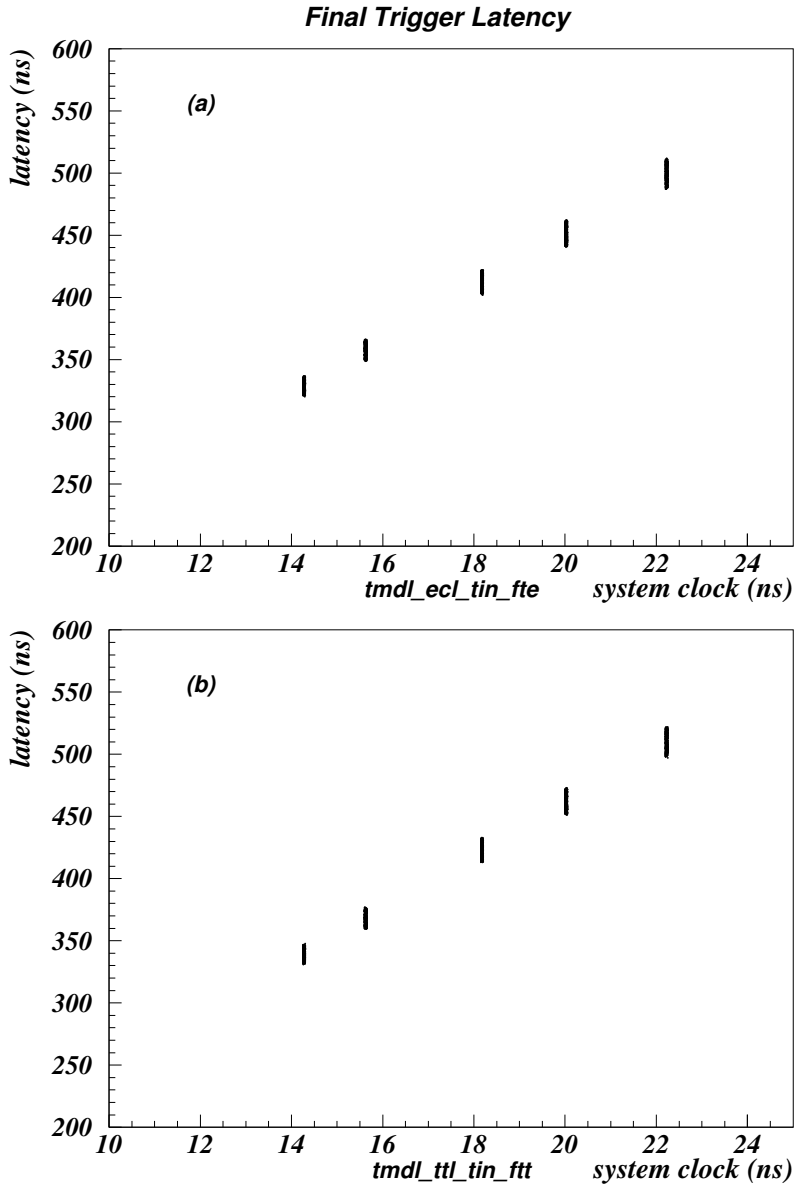

Figure 7.18: Final Trigger Latency (TSC timing to Final Trigger when the trigger type is 0): (a) ECL Final Trigger (b) TTL Final Trigger

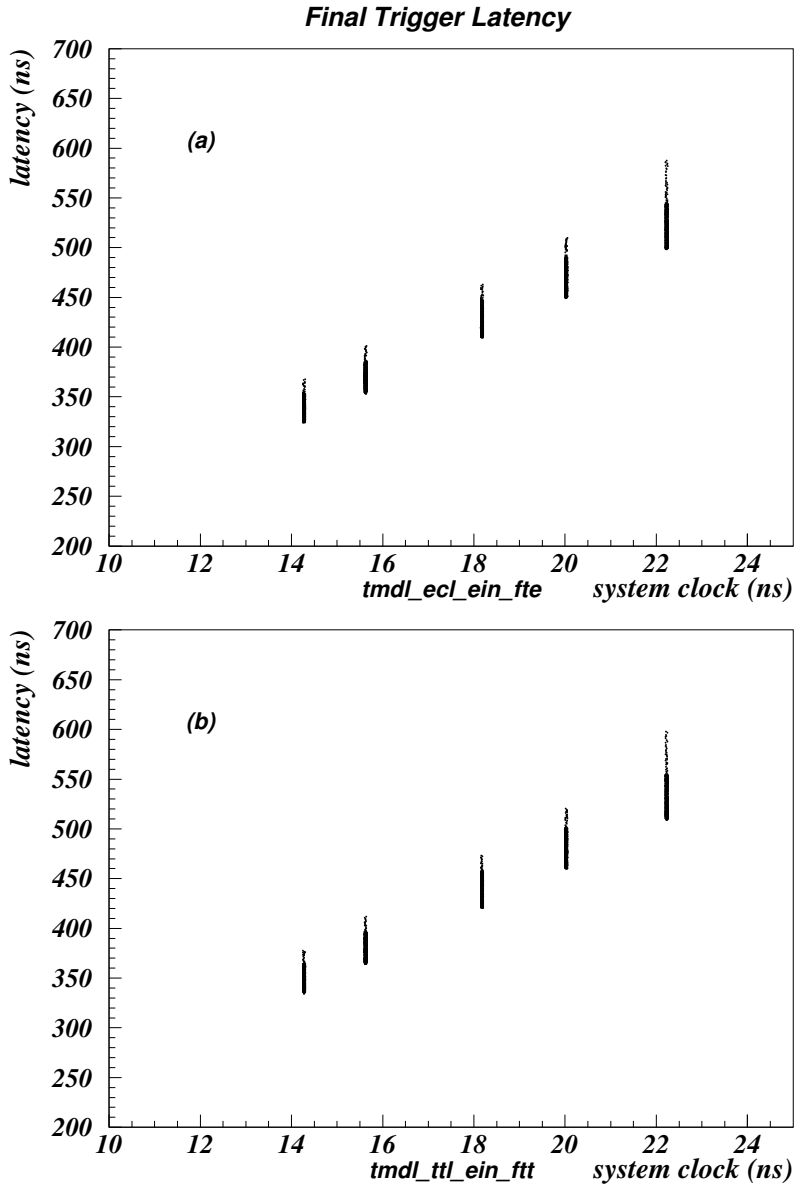

Figure 7.19: Final Trigger Latency (ECL timing to Final Trigger when the trigger type is 1): (a) ECL Final Trigger (b) TTL Final Trigger

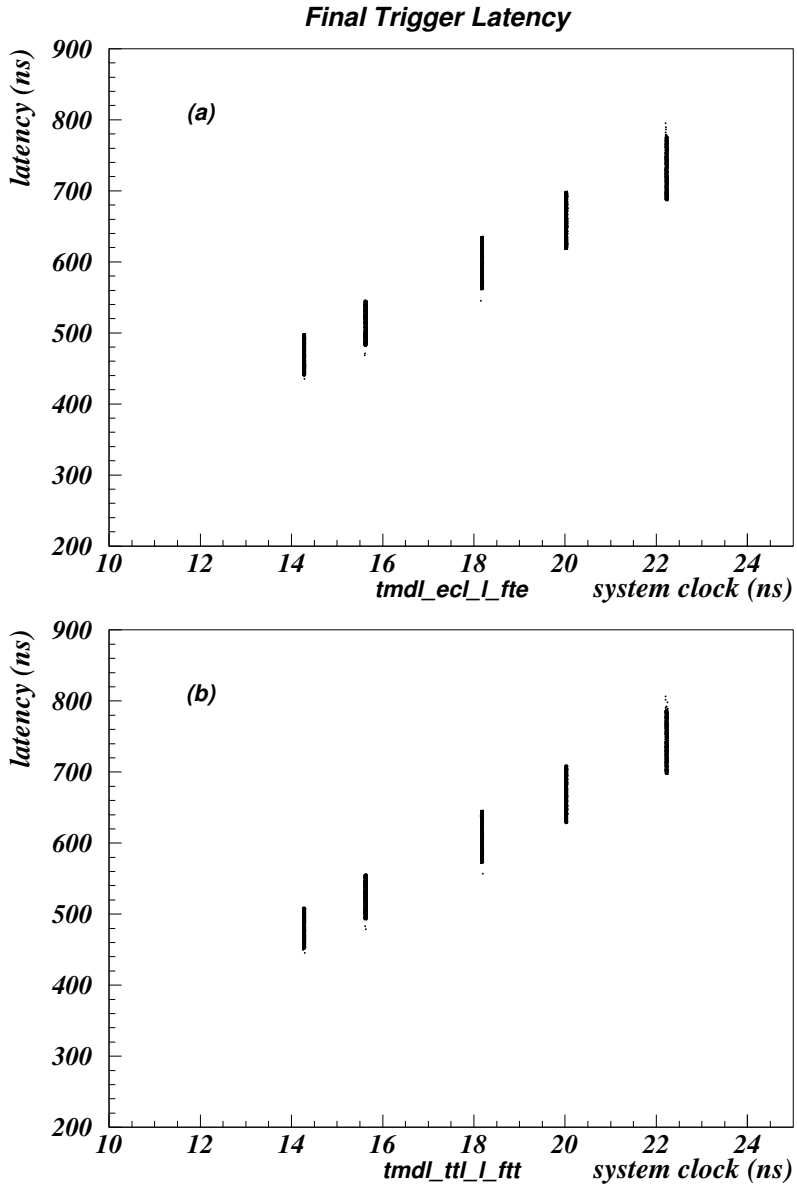

Figure 7.20: Final Trigger Latency (The cue signal to Final Trigger when the trigger type is 2): (a) ECL Final Trigger (b) TTL Final Trigger

Table 7.4: TMDL disallowed ratio

clock [MHz]	ECL final trigger	TTL final trigger
70	1.04%	1.01%
64	1.00%	0.97%
55	1.05%	1.11%
50	1.15%	1.23%
45	1.26%	1.30%

doesn't appear in case of trigger type 0 (TSC timing). Therefore, it seems that there is a loophole in the design. This is thought because of the asynchronousity of the three different frequency system clocks (64MHz, 32MHz, 16MHz). This loophole should be studied more and should be removed.

Minimum Input Pulse Width Efficiency to latch the timing signal is measured with 64MHz system clock, i.e. 64MHz for TSC and 32MHz for ECL. Figure 7.21 shows the the mislatch ratio vs the input pulse width. Since the inputs are converted from ECL to TTL in TMDL module, there is an offset in the graph, again. In order to latch safely, the width of TSC timing signal should be greater than 17.5 ns (probability of failure $(5 \pm 5) \times 10^{-6}$), and the width of ECL timing signal should be greater than 31.3ns (probability of failure $< 1.5 \times 10^{-5}$ CL 95%).

7.5 Summary and Consideration

The performance is summarized in the table 7.5. As to the input signal width margin, only several nano seconds are required and this can be easily satisfied.

As to the maximum system clock, all modules work faster than the planned frequency. However, PSNM can only work with 34 MHz system clock. This is much slower, comparing to other modules. This characteristics arrised from the Xilinx chip property[1].

[1]Refer to *ref.* [15] for details.

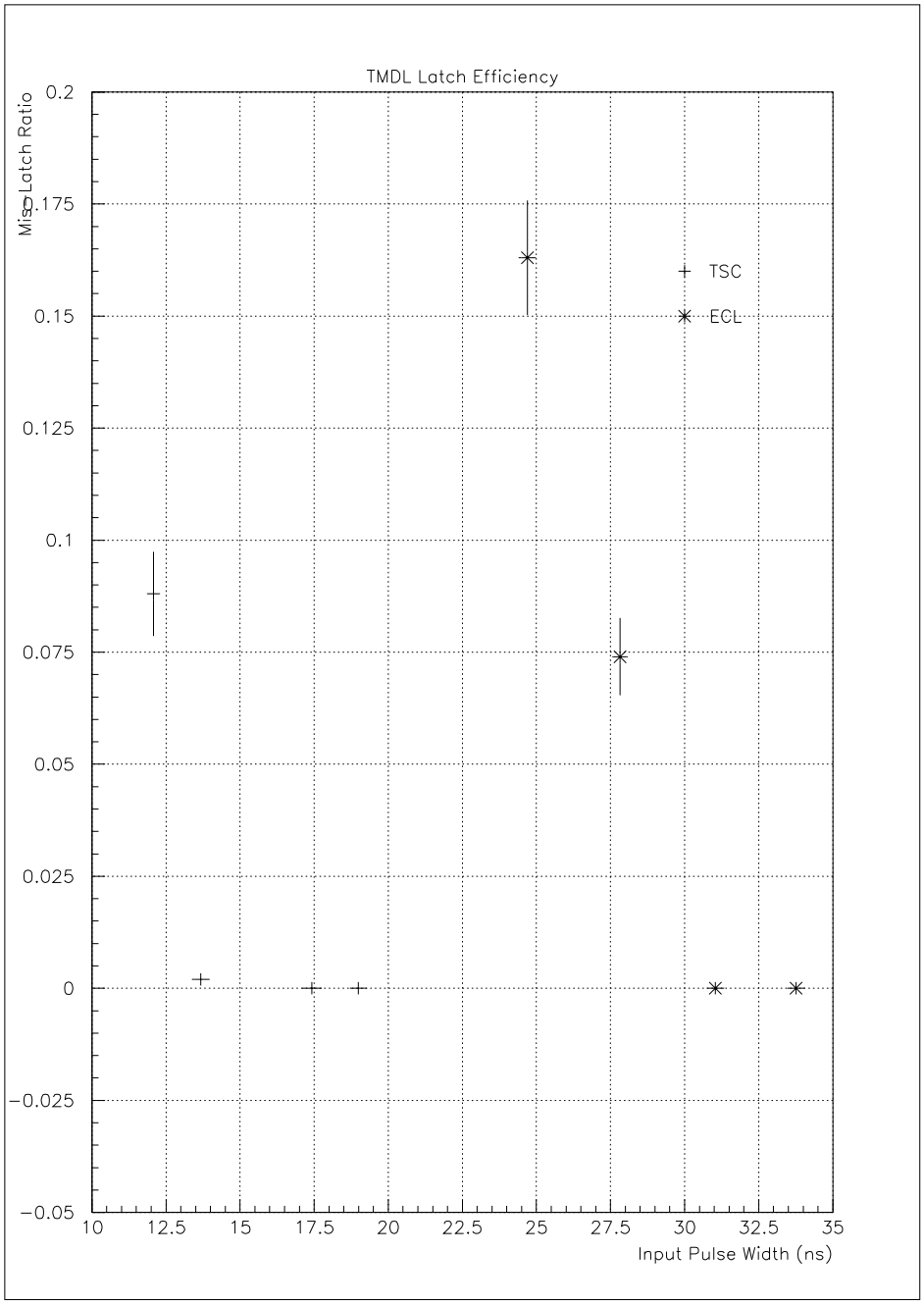

Figure 7.21: Timing Signal Latch Efficiency

Table 7.5: Module Performance Summary

1. for synchronous input
2. for the final trigger with TSC timing

Module	Xilinx chip	Input		System Clock	
		receiver	width margin	max	planned
ITD	XC3130-125PC68	MC10125	1 ns	85 MHz	64/32 MHz
FTDL	XC95108-15PQ160	Xilinx	2∼3 ns	80 MHz	32 MHz
PSNM	XC3190A-09PP175	Xilinx	0 ns[1]	34 MHz	32 MHz
TMDL	XC95108-7PQ160	MC10125	2 ns	70 MHz[2]	64 MHz

When some complicated design is implemented, the parameter which limits the operating frequency of the chip is, not the internal operating frequency of the logical unit cell, but the number of inputs to the unit cell and the delay between unit cells.

In the PSNM case, the unit cell of the XC3190 chip is called as CLB (configurable logic block), which has two flip-flops and allows basically 5 inputs. Since the design of PSNM logic is complicated, it requires many CLB's to implement the design. In order to combine CLB's, the wide interconnect area of FPGA is used. Since the constraint put to the routing in the interconnect area was to limit the net delay between flip-flops just less than 30ns[2], the maximum clock just goes upto 34MHz.

On the other hand, in the case of FTDL, the minimal unit of XC95108, called as macrocell, has one flip-flop. 18 macrocells compose a FB (function block), together with programmable AND-array and product term allocators. This FB allows 36 inputs from the routing resource called FastCONNECT Switch Matrix. Owing to the product term allocators, upto 15 product terms can be available to a single macrocell with only a small incremental delay of t_{PTA}[3]. Further, all 90 product terms are available to any macrocell, with a maximum incremental delay of 8 t_{PTA}. Thanks to these

[2]Putting the constraint as, for example, less than 28ns, the max clock might go upto 36MHz, but anyway this is almost utmost.

[3]t_{PTA} is 2ns for XC95108-15 and -10; 1.5ns for XC95108-7.

flexibly available gates, in spite of the fact that the FTDL is the bulk of AND/OR gates, all related flip-flops could be put spanning only two FB's, therefore the timing simulator guaranteed the operating frequency at least upto f_{SYSTEM}, which is 55MHz for XC95108-15.

Chapter 8

Summary and Future Prospects

The goal for this paper is to design, produce, and check the performance of the BELLE central trigger system GDL. The GDL is designed separately into several functions and implemented, using the technique of FPGA and CPLD, into single width 6U VME modules. Main function modules are called ITD, FTDL, PSNM and TMDL. Performance of these main modules was checked one by one and it turned out to work as designed. Namely, receiving subtriggers from each detector subsystem at t=1.85μs, GDL will provide the final trigger at t=2.2μs, according to its event type. It is confirmed that the trigger efficiency for physics events will not be lost while GDL processing.

In this paper, basically, each module is checked with asynchronous input, and confirmed that these modules work individually, for any relative phase of the input signal and the system clock. As the next step, all modules should be integrated and the performance should be checked as a whole GDL system. The greatest difficulty while making a large synchronous system is to control the relative phase of the system clock and the signal transferred between modules. This phase is controled by changing the propagation delay between modules. Only when the relative phase is adjusted so that the signal will surely latched at the first flip-flop of the downstream module, the system can work. The integration of ITD, FTDL and PSNM is expected to be relatively easy, because they work with 32MHz clock. The combination, on the other hand, of ITD and TMDL, which work with 64MHz clock, is expected to be more difficult, and should be treated carefully. The GDL construction schedule is as shown in the table 8.1.

Since the cross-section becomes smaller and smaller, as the energy goes

Table 8.1: Construction Schedule of GDL

	-	Apr 2Q	Each function modules are checked up completely
Apr 3Q	-	May 3Q	Integration of GDL
May 4Q	-	Jun 4Q	Move to the Electronics Hut; Durability Check
Jun 4Q	-	Jul	Integration with Subtrigger systems

higher, we have to struggle with enormous high event rate in order to do particle physics from now on. On the other hand, the silicon industry is now growing in marvelous speed; and the degree of accumulation of transistor in a programmable device is increasing limitlessly, also speed of chip is getting faster and faster. Thus, the trigger will be able to do much complicated thing in near future. I think this is one of the innovation which is necessary to do high energy physics in future.

Acknowledgements

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I specially thank Ms. M.Yokoi (Nara wu.) and Ms. M.Sasaki (Nara wu.) for drawing the cartoon.

Appendix A

Programmable Logic Device

In these days, programmable logic devices are indispensable for our trigger modules. Among them, FPGA and CPLD are preferable because of their easiness to design; it does not require long turn around time and we can obtain working device right after finishing the design. In this paper Xilinx FPGA (3190A) and CPLD (95108) are used [15]. In this section, where and how they should be used is described.

3190A contains total 928 flip-flops and 95108 contains only 108. Larger chip, 95216 is available now, yet it contains only 216. So, FPGA is better for those which consumes many flip-flops. In GDL, FPGA's are used for ITD, PSNM and Scaler from this reason.

As to FTDL, it requires flip-flops only to latch the inputs and outputs[1], and the main logic part is just and/or gates. So there is no strong preference between FPGA and CPLD for FTDL. Actually CPLD is used in this paper, but we could easily implement it in FPGA.

Difficulty arises with TMDL. CPLD is easy to estimate its propagation delay inside, and is said to be good for a state machine, generally. TMDL is a state machine, but with shift registers. Since the time window is definitely 350ns, it requires 22 bit shift register with 64MHz clock. Inside of CPLD is devided into several function blocks (FB) and each function block has 18 macrocells, which contains product terms and one flip-flop. And this function blocks are connected by switch matrix. So the 18 flip-flops are, in a sense, the maximal unit. Of course it's possible to design using flip-flops beyond

[1]Supposing that there's no need to enlarge the veto signal width.

18. But, in that case, the propagation delay between flip-flops in different FB's becomes so large, and this will limit the maximum internal operating frequency of the design. According to the data sheet, the maximum internal operating frequency within one FB is 125MHz for 95108-7, 111MHz for -10, and if it spreads over two FBs, 83MHz for -7 and 67MHz for -10. And according to the agency of Xilinx, it goes further worse if it expands over more and more FBs. The more compact, the quicker the system can run. TMDL needs two shift registers for TSC timing signal and ECL timing signal. Implementing both of them with 22 bit shift register and making them work with 64MHz is impossible. Thus, the number of steps of the shift register for ECL signal is reduced[2] into half and 32MHz clock is used for that part. It means the preciseness of the final trigger with the ECL timing gets loose, but the ECL timing signal has large jitter intrinsically, so it will not do harm for the final trigger timing, essentially. From the same reason, the internal timer in order to assert the final trigger with the timing of cue signal, etc. is changed to use 16MHz clock. Therefore, in the current design, total 73 flip-flops in TMDL are managed to work with corresponding clocks. Below is the point to implement TMDL into 95108. This will help generally when one implements some large bunch of flip-flops into CPLDs. Note that the Viewlogic and XAbel is used to design CPLD, which is going to be outdated.

- Add the *fast* attribute to the critical pad. The signal line of this attribute does not stay in low power mode, and give good performance instead.
- Compile once without locking the pin location.
- Check the *.xff* file to see the flip-flop name.
- Check the *.gyd* file to see what is in which FB.
- Lock the pin according to the *.gyd* location report.
- Edit *.cst* file using the name checked in *.xff* file.
- Compile again, using the constraint of pin location and timing.

[2]There was another way, not to reduce the number of shift register bits but to implement into a larger chip, i.e. 95216. But 95216 does not have the speed grade -7 so far, so I did not go for that way.

Appendix B

Design of Boards and Programmable chips

B.0.1 FTDL

Figures B.1,B.2 are the electric schematic of the FTDL board. Figures B.3,B.4 are the ViewLogic schematic of the Final Trigger Decision Logic. Figures B.5,B.6 are the ViewLogic schematic for the VME interface part. And below is the XAbel source file, which is used as the symbol "VME" in the figure B.5.

```
MODULE vme

title 'VME interface'

declarations

"logic levels
        H,L,X,VCC,GND = 1,0,.X.,1,0;

"input pins ------------------------------------------------------------------
        A1,A2,A3,A4,A5,A6,A7,A8         pin;    "address (A8 is not used)
        AM0,AM1,AM2,AM3,AM4,AM5         pin;    "address modifiers
        WRITE                           pin;    "write/read
        SYSRES                          pin;    "sytem reset
        IACK                            pin;    "interrupt acknowledge
        MS0,MS1                         pin;    "address16-23match,24-31match
        AS,DS0,DS1                      pin;    "strobes
        DLAY1,DLAY2,DLAY3,DLAY4,DLAY5   pin;    "50,100,150,200,250nsec delayed DELAYIN
"output pins -----------------------------------------------------------------
```

```
        BDTACK                          pin;    "Data Acknowledge
        BBERR                           pin;    "Bus Error
        DELAYIN                         pin;    "to Active Delay Input
        SS1,DIR                         pin;    "for 74LS645
        RSTAT,WCTRL,CLKSL,PROGX,TDITM   pin;    "for XC95108PQ160 programming
        REGADDR,SEQCTRL                 pin;    "to control DATA RAM
"clock out ------------------------------------------------------------------------

"vector definitions
        AMCODE = [AM5,AM4,AM3,AM2,AM1,AM0];
        ADDR   = [A7,A6,A5,A4,A3,A2,A1,X];

"internal nodes (pins also)
        U24,S24,U32,S32                 node;   "AM code
        SELECT                          pin;    "Module Selected
        REG0                            pin;
        REG1,REG2,REG3,REG4             pin;
        REG5,REG6,REG7,REG8             pin;
        REG9,REGA,REGB,REGC             pin;
        REGD,REGE,REGF                  pin;
        RSL,RSH,WSL,WSH                 pin;    "r/w strobes for upper/lower bits

"end of declarations

equations

"address
        SELECT = ((S32 # U32) & !MS0 & !MS1 # (S24 # U24) & !MS0) & !AS & IACK;

"address modifier
        S24 = (AMCODE==^h3E)#(AMCODE==^h3D);
        U24 = (AMCODE==^h3A)#(AMCODE==^h39);
        S32 = (AMCODE==^h0E)#(AMCODE==^h0D);
        U32 = (AMCODE==^h0A)#(AMCODE==^h09);

"data strobe
        RSL = WRITE & SELECT & !DS0;
        RSH = WRITE & SELECT & !DS1;
        WSL = !WRITE & SELECT & !DS0;
        WSH = !WRITE & SELECT & !DS1;

"250ns active delay
        DELAYIN = !DS0 # !DS1;
```

```
"data acknowledge / buss error
        BDTACK = !WRITE & SELECT & DLAY3 & (!DS0 # !DS1) # WRITE & SELECT & DLAY3 & (!DS0 # !
        BBERR = GND;

"74LS645
        SS1 = GND;              "enabled
        DIR = RSL;             "1 for read operation

"system reset
"       SYSRES = ;

"addresss asignment
"256bit VME address space
        RSTAT = SELECT & (ADDR == ^H00);
        WCTRL = SELECT & (ADDR == ^H04);
        CLKSL = SELECT & (ADDR == ^H08);
        PROGX = SELECT & (ADDR == ^H0C);
        TDITM = SELECT & (ADDR == ^H10);

        REGADDR = SELECT & (ADDR == ^H14);
        SEQCTRL = SELECT & (ADDR == ^H18);

        REG0  = SELECT & (ADDR == ^H20);
        REG1  = SELECT & (ADDR == ^H24);
        REG2  = SELECT & (ADDR == ^H28);
        REG3  = SELECT & (ADDR == ^H2C);
        REG4  = SELECT & (ADDR == ^H30);
        REG5  = SELECT & (ADDR == ^H34);
        REG6  = SELECT & (ADDR == ^H38);
        REG7  = SELECT & (ADDR == ^H3C);
        REG8  = SELECT & (ADDR == ^H40);
        REG9  = SELECT & (ADDR == ^H44);
        REGA = SELECT & (ADDR == ^H48);
        REGB = SELECT & (ADDR == ^H4C);
        REGC = SELECT & (ADDR == ^H50);
        REGD = SELECT & (ADDR == ^H54);
        REGE = SELECT & (ADDR == ^H58);
        REGF = SELECT & (ADDR == ^H5C);
"i.e
"       0x00    READ STATUS REGISTER
"                [bit0=PCLOCKSEL,bit1=LEDENABLE,bit2=PROGENABLE,
"                 bit3=TDO,bit4=TDI,bit5=TMS,bit6=GND,bit7=VCC]
"       0X04    WRITE CONTROL REGISTER [Not Used]
"       0X08    SELECT CLOCK / LED CONTROL
```

```
"                [bit0(1:external 0:internal),
"                 bit1(1:enable LEDs 0:disable LEDs)]
"       0X0C    PROGRAM XILINX FROM VME enable[bit0 1=enable]
"       0X10    WRITE TMS[bit0] AND TDI[bit1]
"
"       0x14    REGISTER ADDRESS
"                [bit0-bit3:register address,bit4:LOADREGADDR]
"       0x18    SEQUENSER CONTROL
"                [bit0:AUTOSTOP,bit1:CLKSTART,bit2:CLRREGADDR]
"
"                         7      0
"       0x20    REG0    +--------+
"       0x24    REG1    |  data  |
"                         RAM
"       0x5C    REGF    +--------+
"end of equations

"test vectors

"end of test vectors

END vme
```

Table B.1 is the signal numbering of the inputs.

Table B.1: FTDL Input Signal Numbering

No.	label	No.	label
0	$N_{CDR-full}0$	1	$N_{CDR-full}1$
2	$N_{CDR-short}0$	3	$N_{CDR-short}1$
4	CDC:open	5	$N_{CDZ}0$
6	$N_{CDZ}1$	7	TSC:timing
8	$N_{TSC}0^1$	9	$N_{TSC}1$
10	$N_{TSC}2^1$	11	$N_{TSC}3^1$
12	$E_{tot}0$	13	$E_{tot}1$
14	$E_{tot}2$	15	$N_{icl}0$
16	$N_{icl}1$	17	$N_{icl}2$
18	$N_{icl}3^1$	19	ECL:BB_{pre}
20	ECL:BB	21	ECL:cosmic
22	ECL:timing^1	23	EFC:BB
24	EFC:Tag0	25	CALIB0

Table B.2 shows the test input pattern (I0 to I25). ↑ (↓) means that the leading edge of the input signal is rising (falling) edge. Table B.3 is the signal numbering of the outputs.

Table B.4 shows the test output pattern corresponding to the input pattern I0 to I25. ↑ (↓) means that the leading edge of the input signal is rising (falling) edge.

Table B.2: FTDL Test Input Matrix

I8, I10, I11, I18, I22 are not checked.

Pattern No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
I0	↑	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I1	0	↑	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I2	1	0	↑	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I3	0	0	0	↑	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I4	1	1	1	1	↑	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I5	1	1	1	1	1	↑	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I6	1	1	1	1	1	0	↑	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I7	1	1	1	1	1	1	1	↑	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1
I8	1	1	1	1	1	1	1	1	↑	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I9	1	1	1	1	1	1	1	1	1	↑	0	0	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I10	1	1	1	1	1	1	1	1	1	0	↑	0	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I11	1	1	1	1	1	1	1	1	1	0	0	↑	1	1	1	1	1	1	1	1	0	0	1	1	1	1
I12	1	1	1	1	1	1	1	1	1	1	1	1	↑	1	1	1	1	1	1	1	0	0	1	1	1	1
I13	1	1	1	1	1	1	1	1	1	1	1	1	1	↑	1	1	1	1	1	1	0	0	1	1	1	1
I14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	↑	1	1	1	1	1	0	0	1	1	1	1
I15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	↑	1	0	0	1	0	0	1	1	1	1
I16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	↑	0	0	1	0	0	1	1	1	1
I17	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	↑	0	1	0	0	1	1	1	1
I18	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	↑	1	0	0	1	1	1	1
I19	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	↑	0	0	1	1	1	1
I20	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	↓	0	1	1	1	1
I21	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	↓	1	1	1	1
I22	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	↑	1	1	1
I23	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	↑	1	1
I24	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	↑	1
I25	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	↑

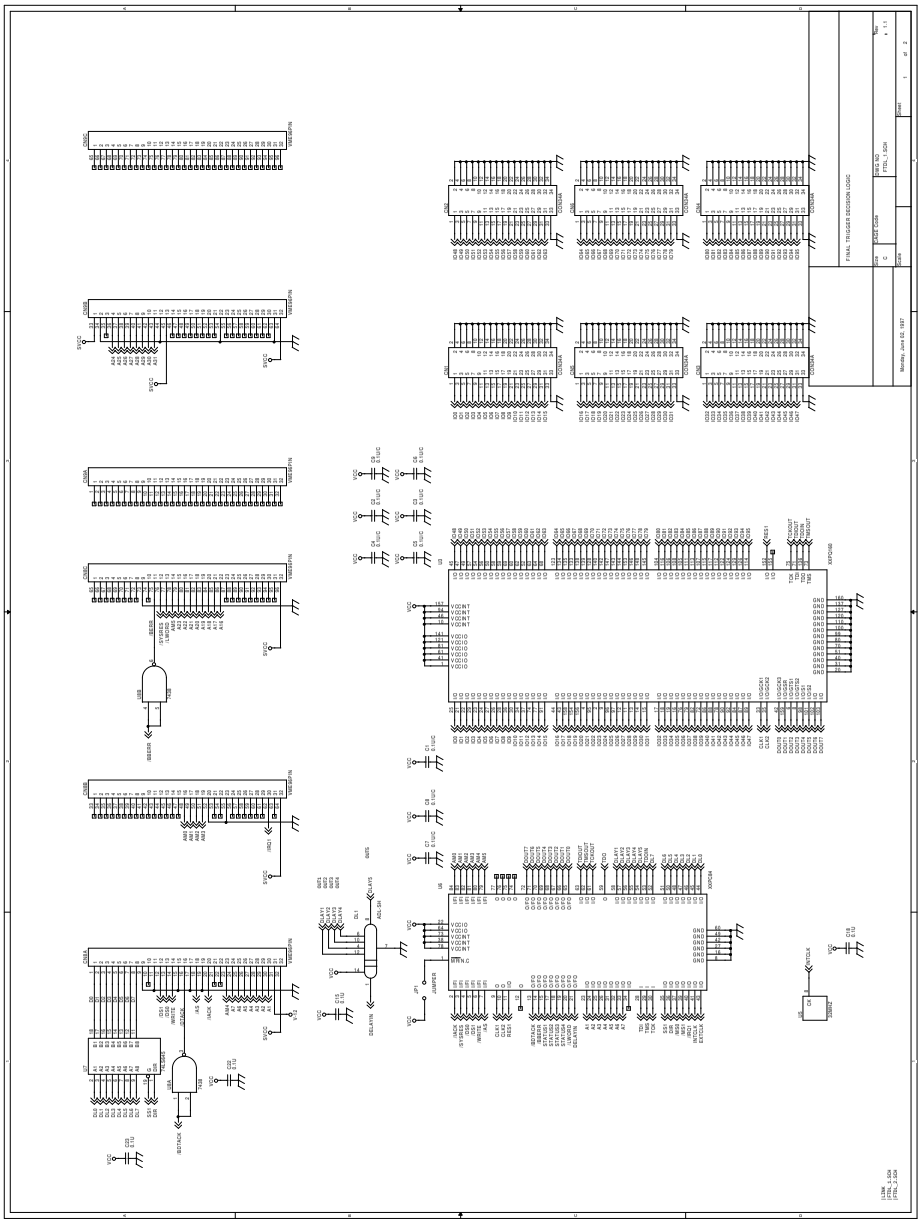


Figure B.1: The Final Trigger Decision Logic Board (page1)

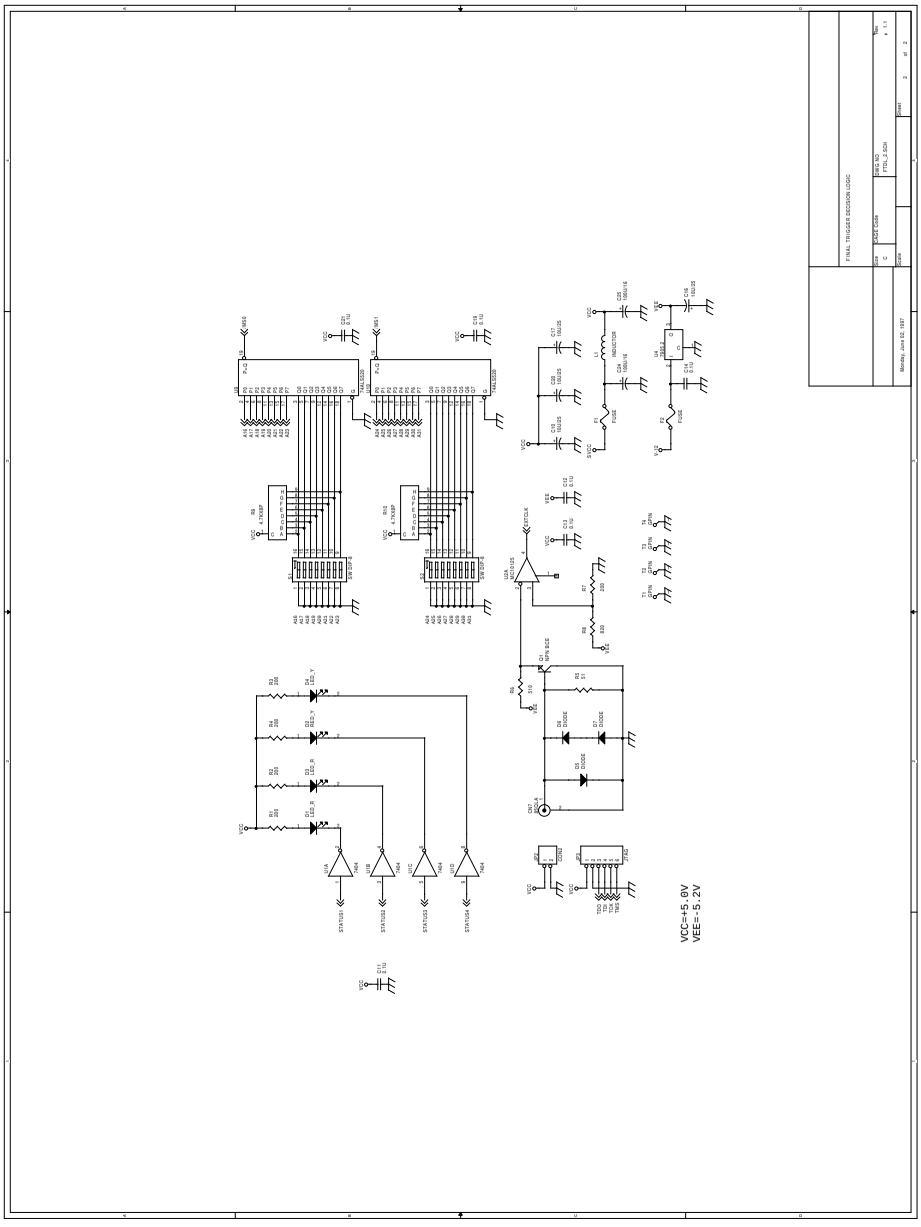


Figure B.2: The Final Trigger Decision Logic Board (page 2)

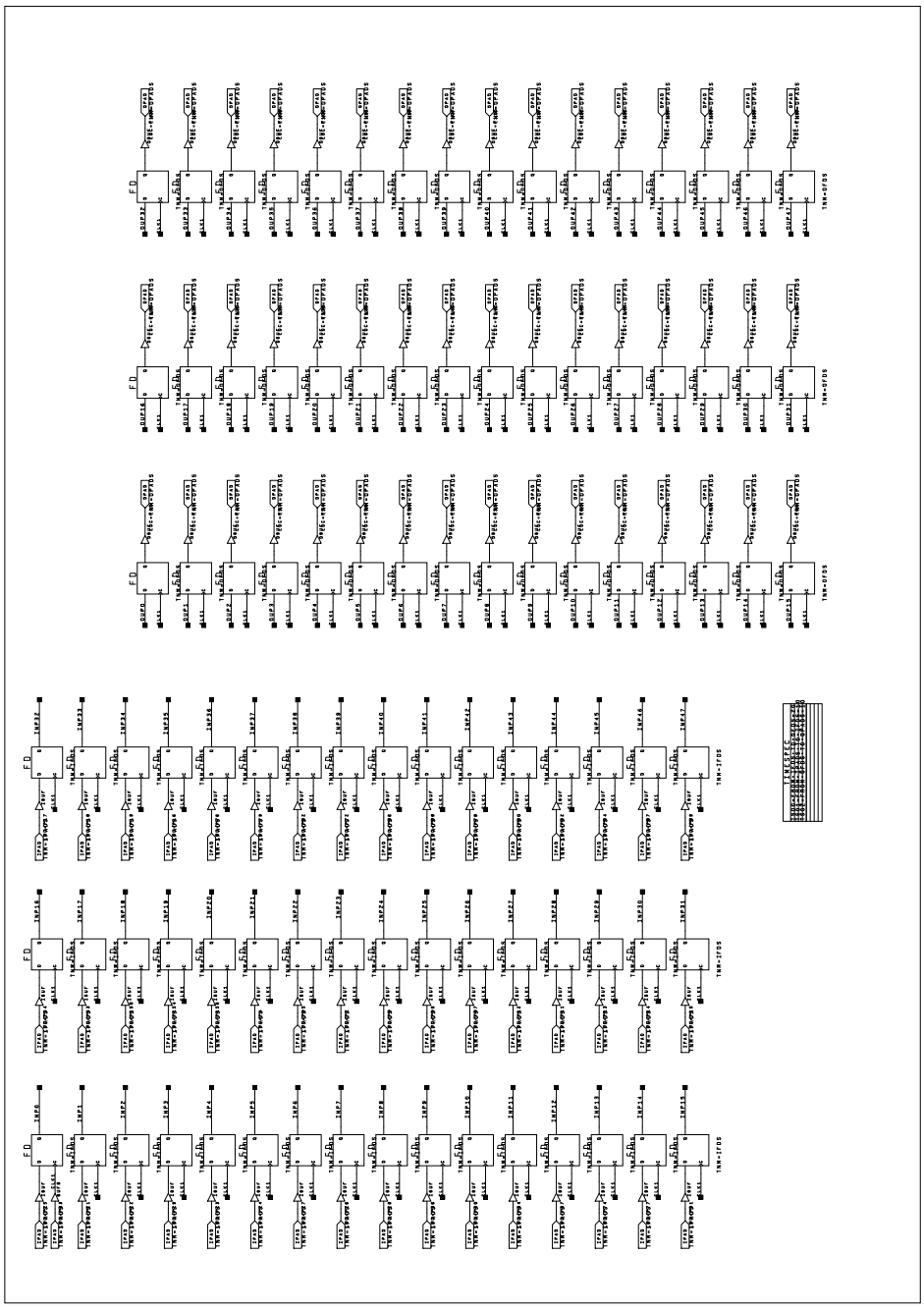


Figure B.3: The Final Trigger Decision Logic (page 1)

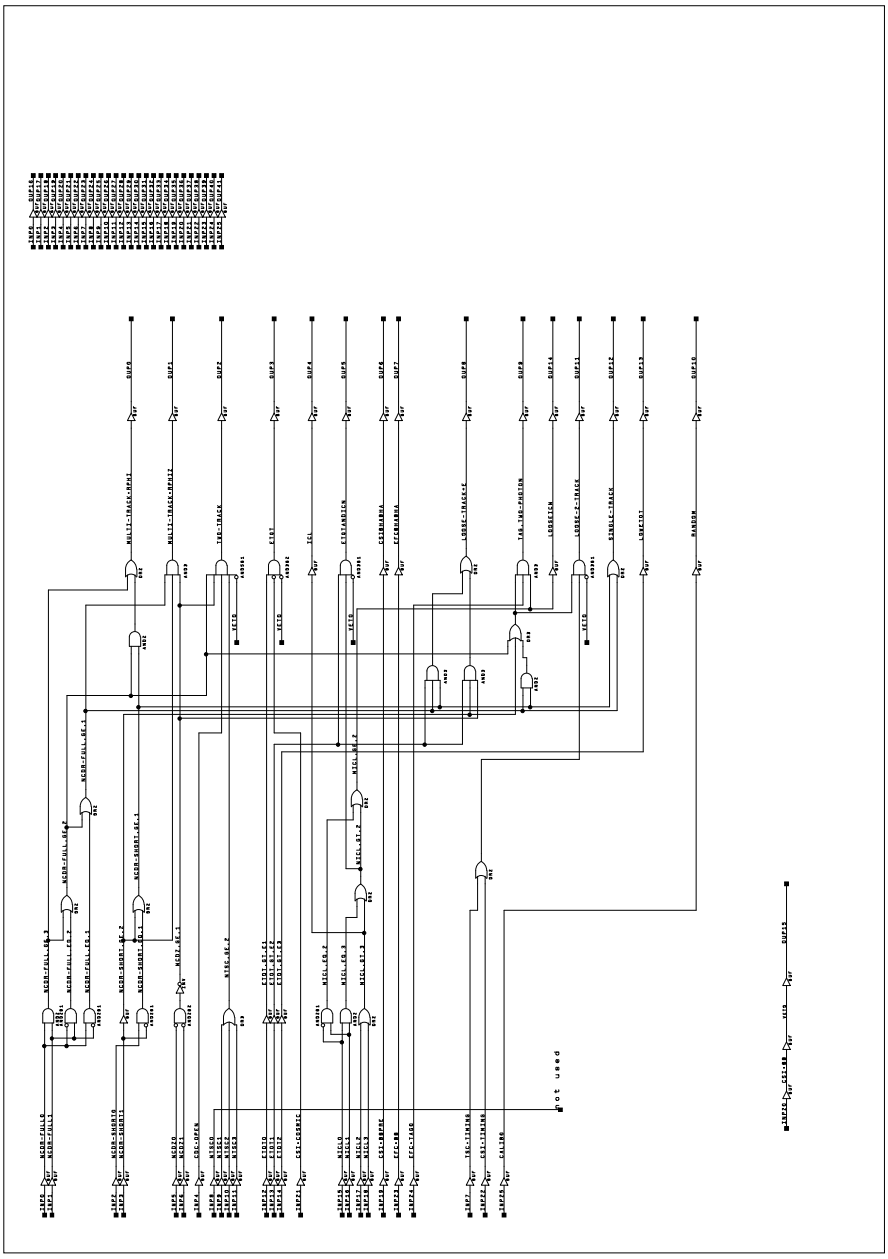


Figure B.4: The Final Trigger Decision Logic (page 2) NOTE : CSI:BB connected to OUP15 is just for debug purpose, and should be removed for the actual use.

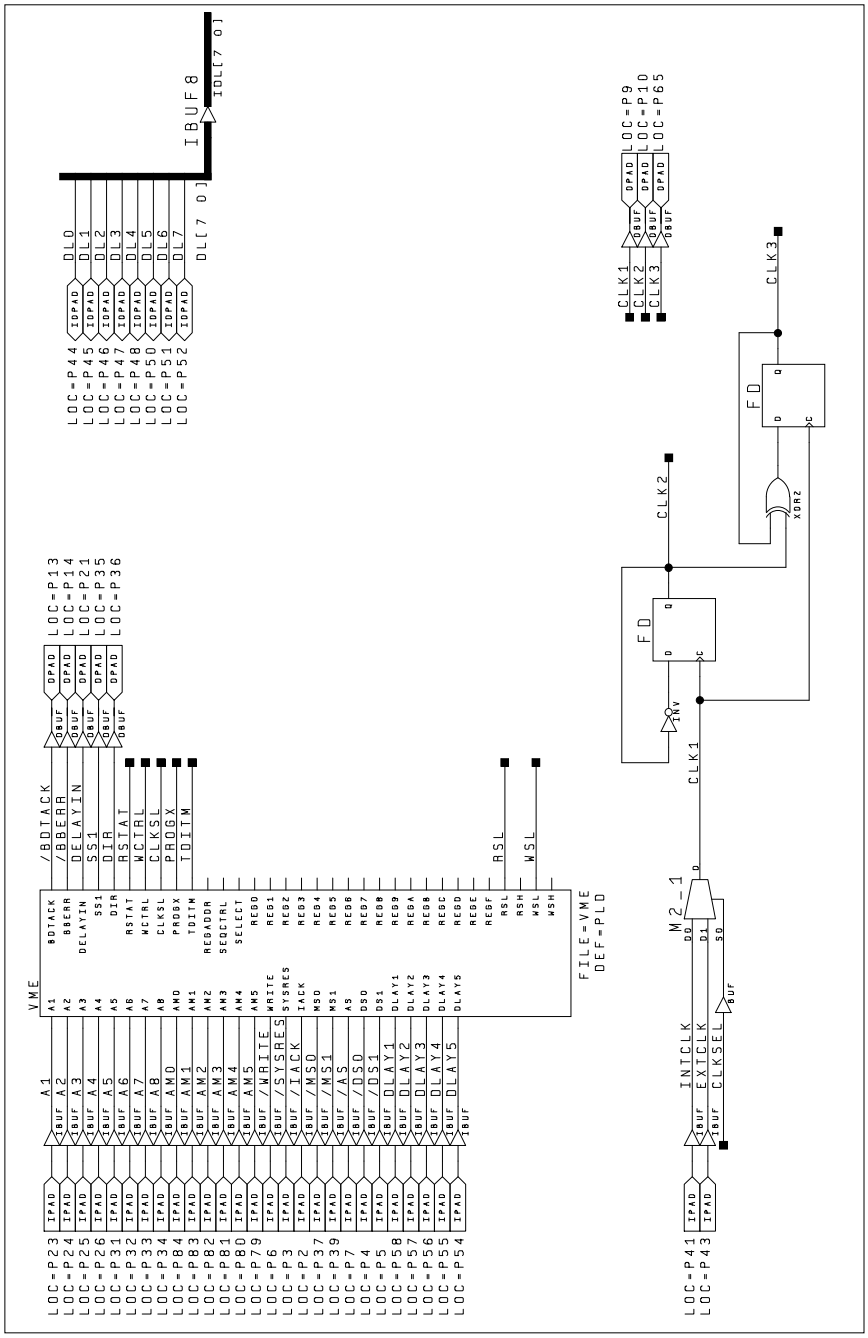


Figure B.5: The VME interface part of Final Trigger Decision Logic Board (page 1)

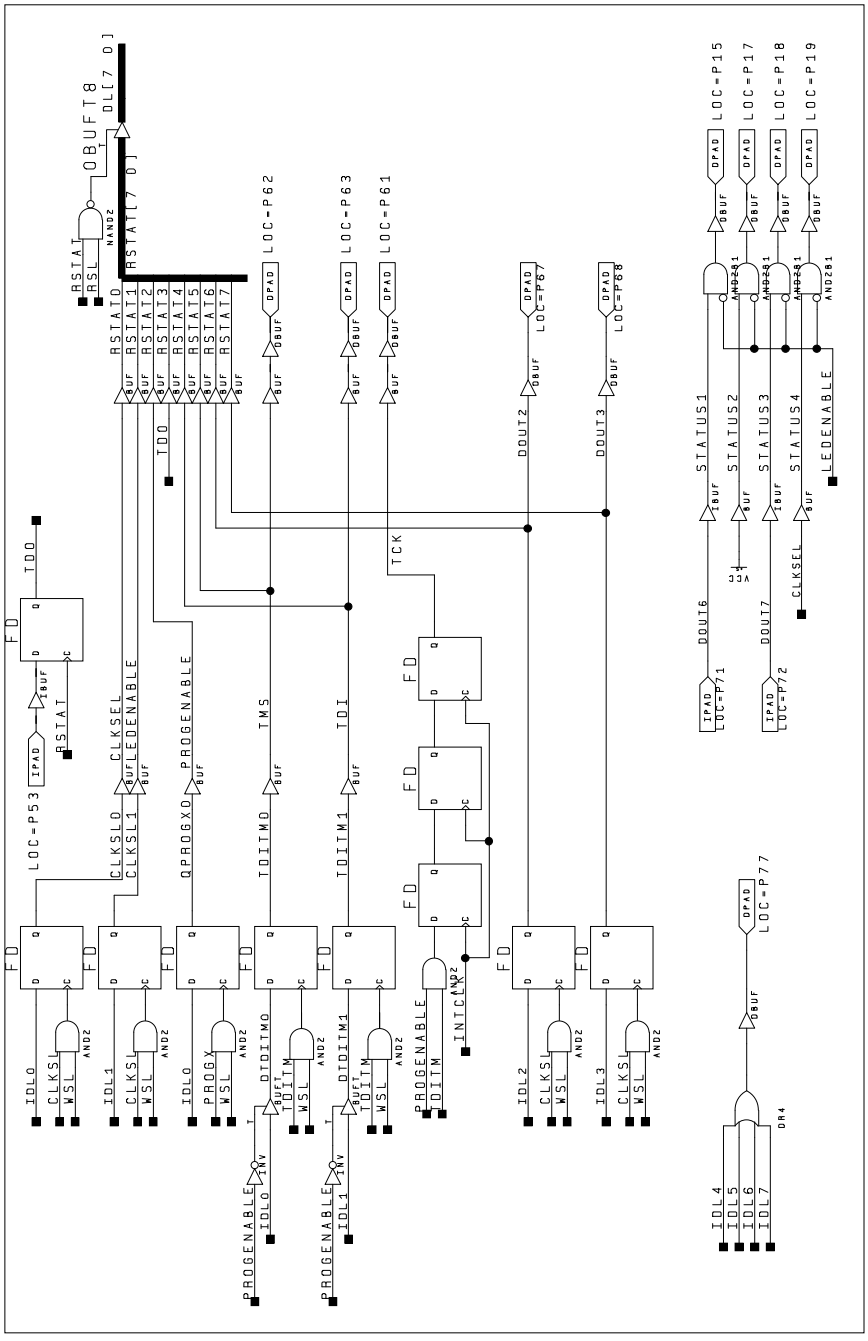


Figure B.6: The VME interface part of Final Trigger Decision Logic Board (page 2)

Table B.3: FTDL Output Signal Numbering

No.	label	No.	label
O0	Multi-Track:Rϕ	O1	Multi-Track:RϕZ
O2	Two-Track	O3	E_{tot}
O4	Isolated Cluster	O5	E_{tot} × ICN
O6	ECL Bhabha	O7	EFC Bhabha
O8	Loose Track × E	O9	Tag Two-photon
O10	Random	O11	Loose 2-Tracks
O12	Single Track	O13	Low E_{tot}
O14	Loose ICN		

B.0.2 PSNM

Figures B.7, B.8, B.9, B.10 are the ViewLogic schematic of the Prescale and Mask Logic. This is for Xilinx chip no. 0, and that for 1 to 3 are different from this only in pin configuration. Bellow are the XAbel source files, which are used as the symbol "MUX5_1" and "SYNCCNTR" in the logic.

```
module MUX5_1

title   'multiplexer 5 into 1 for PSNM with Suehiro module
                07 Sep. 1997    Yutaka USHIRODA  Kyoto univ.'

declarations
"logic levels
        H,L,VCC,GND,X,C,Z = 1,0,1,0,.X.,.C.,.Z.;
"input pins
        SEL4,SEL3,SEL2,SEL1,SEL0        pin;
        IN4, IN3, IN2, IN1, IN0         pin;
"output pins
        OUT                             pin;
"vector definitions
        SEL = [SEL4..SEL0];

equations
        OUT = (SEL == ^H10)&IN4 # (SEL == ^H08)&IN3 # (SEL == ^H04)&IN2 # (SEL == ^H02)&IN1 #

test_vectors
        ([SEL4,SEL3,SEL2,SEL1,SEL0,IN4,IN3,IN2,IN1,IN0] -> [OUT])
```

Table B.4: FTDL I/O Matrix

I8, I10, I11, I18, I22 are not checked.

Pattern No.	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14
I0	0	0	0	1	1	1	1	1	↑	↑	1	↑	1	1	1
I1	↑	0	↑	1	1	1	1	1	↑	↑	1	↑	1	1	1
I2	0	0	0	1	1	1	1	1	↑	↑	1	↑	1	1	1
I3	0	0	0	1	1	1	1	1	↑	↑	1	↑	↑	1	1
I4	1	1	↑	1	1	1	1	1	1	1	1	1	1	1	1
I5	1	↑	↑	1	1	1	1	1	1	1	1	1	1	1	1
I6	1	↑	↑	1	1	1	1	1	1	1	1	1	1	1	1
I7	1	1	1	1	1	1	1	1	1	1	1	↑	1	1	1
I8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
I9	1	1	↑	1	1	1	1	1	1	1	1	1	1	1	1
I10	1	1	↑	1	1	1	1	1	1	1	1	1	1	1	1
I11	1	1	↑	1	1	1	1	1	1	1	1	1	1	1	1
I12	1	1	1	↑	1	1	1	1	1	1	1	1	1	1	1
I13	1	1	1	1	1	↑	1	1	↑	1	1	1	1	1	1
I14	1	1	1	1	1	1	1	1	1	1	1	1	1	↑	1
I15	1	1	1	1	0	↑	1	1	1	1	1	1	1	1	1
I16	1	1	1	1	0	0	1	1	1	↑	1	1	1	1	↑
I17	1	1	1	1	↑	↑	1	1	1	↑	1	1	1	1	↑
I18	1	1	1	1	↑	↑	1	1	1	↑	1	1	1	1	↑
I19	1	1	1	1	1	1	↑	1	1	1	1	1	1	1	1
I20	1	1	↓	↓	1	↓	1	1	1	1	1	↓	1	1	1
I21	1	1	1	↓	1	1	1	1	1	1	1	1	1	1	1
I22	1	1	1	1	1	1	1	1	1	1	1	↑	1	1	1
I23	1	1	1	1	1	1	1	↑	1	1	1	1	1	1	1
I24	1	1	1	1	1	1	1	1	1	↑	1	1	1	1	1
I25	1	1	1	1	1	1	1	1	1	1	↑	1	1	1	1

```
         [  0 ,  0 ,  0 ,  0 ,  0 , 0 , 0 , 1 , 1 , 0 ] -> [ 0 ];
         [  0 ,  0 ,  0 ,  0 ,  1 , 0 , 0 , 1 , 1 , 0 ] -> [ 0 ];
         [  0 ,  0 ,  1 ,  0 ,  1 , 0 , 1 , 1 , 0 , 1 ] -> [ 0 ];
         [  0 ,  0 ,  0 ,  1 ,  0 , 1 , 0 , 1 , 1 , 1 ] -> [ 1 ];
"end test_vectors

end MUX5_1


module syncccntr
title 'arbitrary length counter with carry out for PSNM with FPGA
        Yutaka USHIRODA Kyoto University
        14 Sep 1997
        07 Jan 1998 modified for PSNM ver.3'

declarations
"logic levels
        H,L,X,VCC,GND,C = 1,0,.X.,1,0,.C.;
"input pins
        P0,P1,P2,P3             pin;    "prescale value
        P4,P5,P6,P7             pin;    "prescale value
        CLOCK                   pin;    "clock
        CE_BAR,CLR              pin;    "CE=0:enable,CLR=1:clr
"output pins
        C0,C1,C2,C3             pin istype 'REG';
        C4,C5,C6,C7             pin istype 'REG';
        TO                      pin istype 'REG';
        MASKOUT                 pin;    "active 1
"        THROUGH                 pin;
"vector definitions
        PSVAL = [P7..P0];
        COUNT = [C7..C0];

equations
@alternate
        MASKOUT = (PSVAL == ^h 00);
"        THROUGH = (PSVAL == ^h 01);

        TO.CLK = CLOCK;
        TO.ACLR= CLR;
        COUNT.CLK = CLOCK;
        COUNT.ACLR= CLR;

        C0 := CE_BAR * C0 + /CE_BAR * /TO * (C0 :+: 1);
```

```
        C1 := CE_BAR * C1 + /CE_BAR * /TO * (C1 :+: C0);
        C2 := CE_BAR * C2 + /CE_BAR * /TO * (C2 :+: C0*C1);
        C3 := CE_BAR * C3 + /CE_BAR * /TO * (C3 :+: C0*C1*C2);
        C4 := CE_BAR * C4 + /CE_BAR * /TO * (C4 :+: C0*C1*C2*C3);
        C5 := CE_BAR * C5 + /CE_BAR * /TO * (C5 :+: C0*C1*C2*C3*C4);
        C6 := CE_BAR * C6 + /CE_BAR * /TO * (C6 :+: C0*C1*C2*C3*C4*C5);
        C7 := CE_BAR * C7 + /CE_BAR * /TO * (C7 :+: C0*C1*C2*C3*C4*C5*C6);

        TO := (COUNT == (PSVAL - 1)) * /CE_BAR + TO * CE_BAR;

test_vectors
        ([CLOCK,CLR,CE_BAR,PSVAL] -> [TO,COUNT])
         [  C  , 0 ,   0   ,  4  ] -> [ 0,  1  ];
         [  C  , 0 ,   0   ,  4  ] -> [ 0,  2  ];
         [  C  , 0 ,   0   ,  4  ] -> [ 1,  3  ];
         [  C  , 0 ,   0   ,  4  ] -> [ 0,  0  ];
         [  C  , 0 ,   0   ,  4  ] -> [ 0,  1  ];
         [  X  , 1 ,   X   ,  X  ] -> [ 0,  0  ];
         [  C  , 0 ,   0   ,  5  ] -> [ 0,  1  ];
         [  C  , 0 ,   0   ,  5  ] -> [ 0,  2  ];
         [  C  , 0 ,   0   ,  5  ] -> [ 0,  3  ];
         [  C  , 0 ,   0   ,  5  ] -> [ 1,  4  ];
         [  C  , 0 ,   0   ,  5  ] -> [ 0,  0  ];
         [  C  , 0 ,   0   ,  5  ] -> [ 0,  1  ];
         [  X  , 1 ,   X   ,  X  ] -> [ 0,  0  ];
         [  C  , 1 ,   0   , 100 ] -> [ 0,  0  ];

@const i=1; @repeat 96 {
         [  C  , 0 ,   0   , 100 ] -> [ 0,@expr i;]; @const i=i+1;}

         [  C  , 0 ,   0   , 100 ] -> [ 0, 97  ];
         [  C  , 0 ,   0   , 100 ] -> [ 0, 98  ];
         [  C  , 0 ,   0   , 100 ] -> [ 1, 99  ];
         [  C  , 0 ,   1   , 100 ] -> [ 1, 99  ];
         [  C  , 0 ,   0   , 100 ] -> [ 0,  0  ];

"end test_vectors
end synccntr
```

B.0.3 TMDL

Figures B.11,B.12 are the electric schematic of the TMDL board. Figures B.13,B.14 are the ViewLogic schematic for the VME interface part. And below is the XAbel source file, which is used as the symbol "VME_T" in the figure B.13.

```
MODULE vme_t

title 'VME interface for TMDL
        1997.12.11      Yutaka USHIRODA  Kyoto univ.'

declarations

"logic levels
        H,L,X,VCC,GND = 1,0,.X.,1,0;

"input pins ------------------------------------------------------------------
        A1,A2,A3,A4,A5,A6,A7            pin;    "address
        AM0,AM1,AM2,AM3,AM4,AM5         pin;    "address modifiers
        WRITE                           pin;    "write/read
        IACK                            pin;    "interrupt acknowledge
        MS0,MS1,MS2                     pin;    "address8-16,16-23,24-31match
        AS,DS0,DS1                      pin;    "strobes
        DLAY1,DLAY2,DLAY3,DLAY4,DLAY5   pin;    "50,100,150,200,250nsec delayed DELAYIN
"output pins -----------------------------------------------------------------
        BDTACK                          pin;    "Data Acknowledge
        BBERR                           pin;    "Bus Error
        DELAYIN                         pin;    "to Active Delay Input
        DIR                             pin;    "for 74LS645
        RSTAT,WCTRL,COMMAND,PROGX,TDITM pin;    "for XC95108PQ160 programming
"clock out -------------------------------------------------------------------

"vector definitions
        AMCODE = [AM5,AM4,AM3,AM2,AM1,AM0];
        ADDR   = [A7,A6,A5,A4,A3,A2,A1,X];

"internal nodes (pins also)
        U24,S24,U32,S32                 node;   "AM code
        SELECT                          pin;    "Module Selected
        RSL,RSH,WSL,WSH                 pin;    "r/w strobes for upper/lower bits

"end of declarations

equations
```

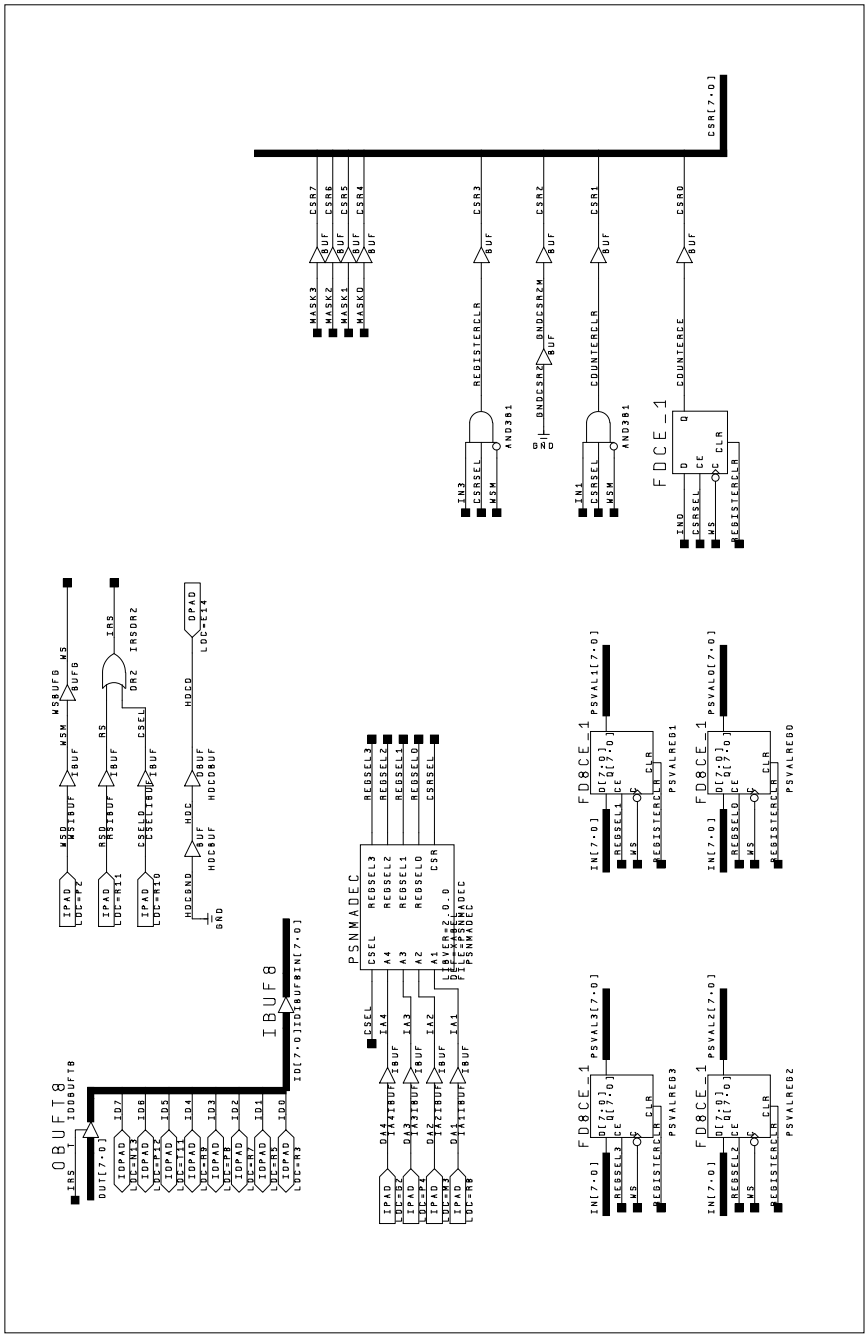


Figure B.7: The Prescale and Mask Logic (page 1)

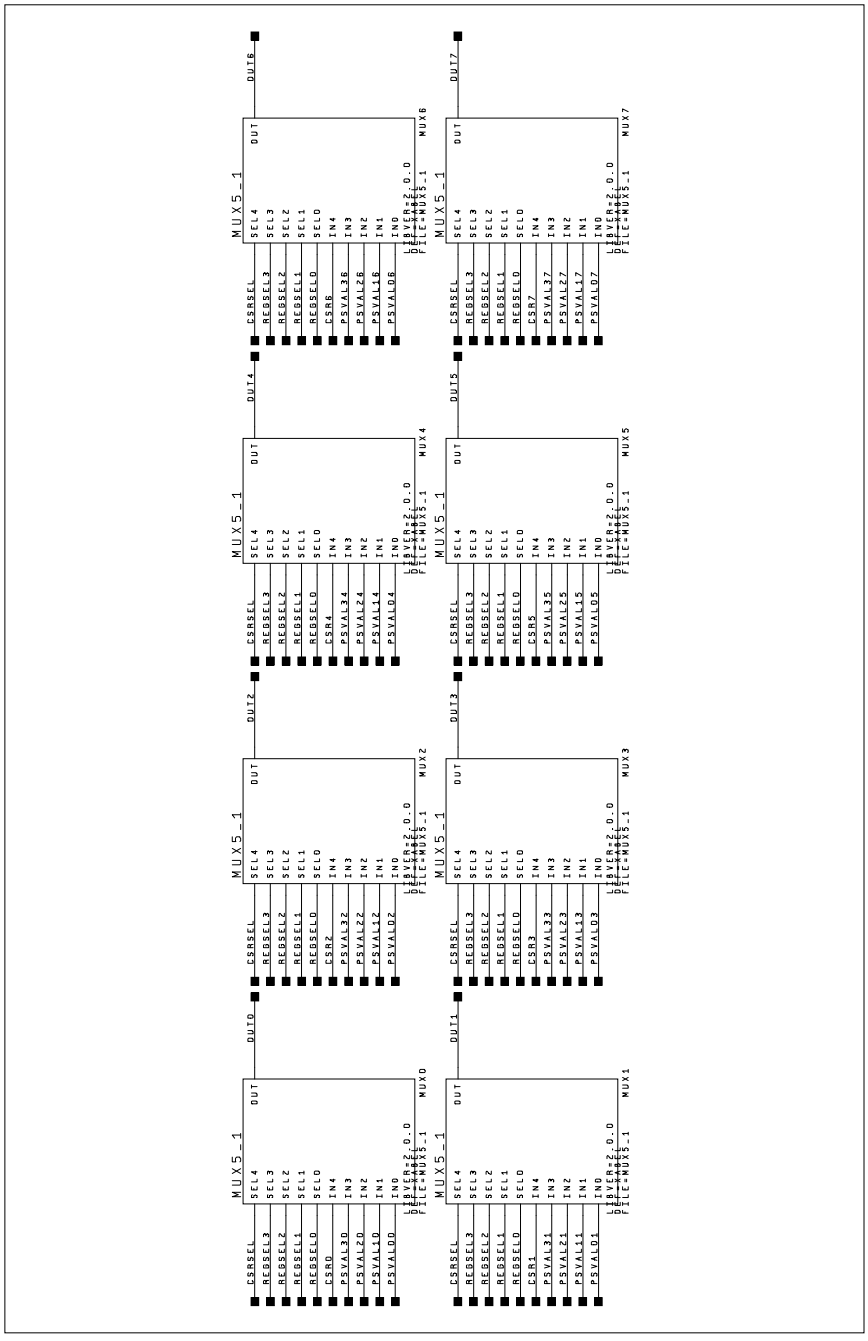


Figure B.8: The Prescale and Mask Logic (page 2)

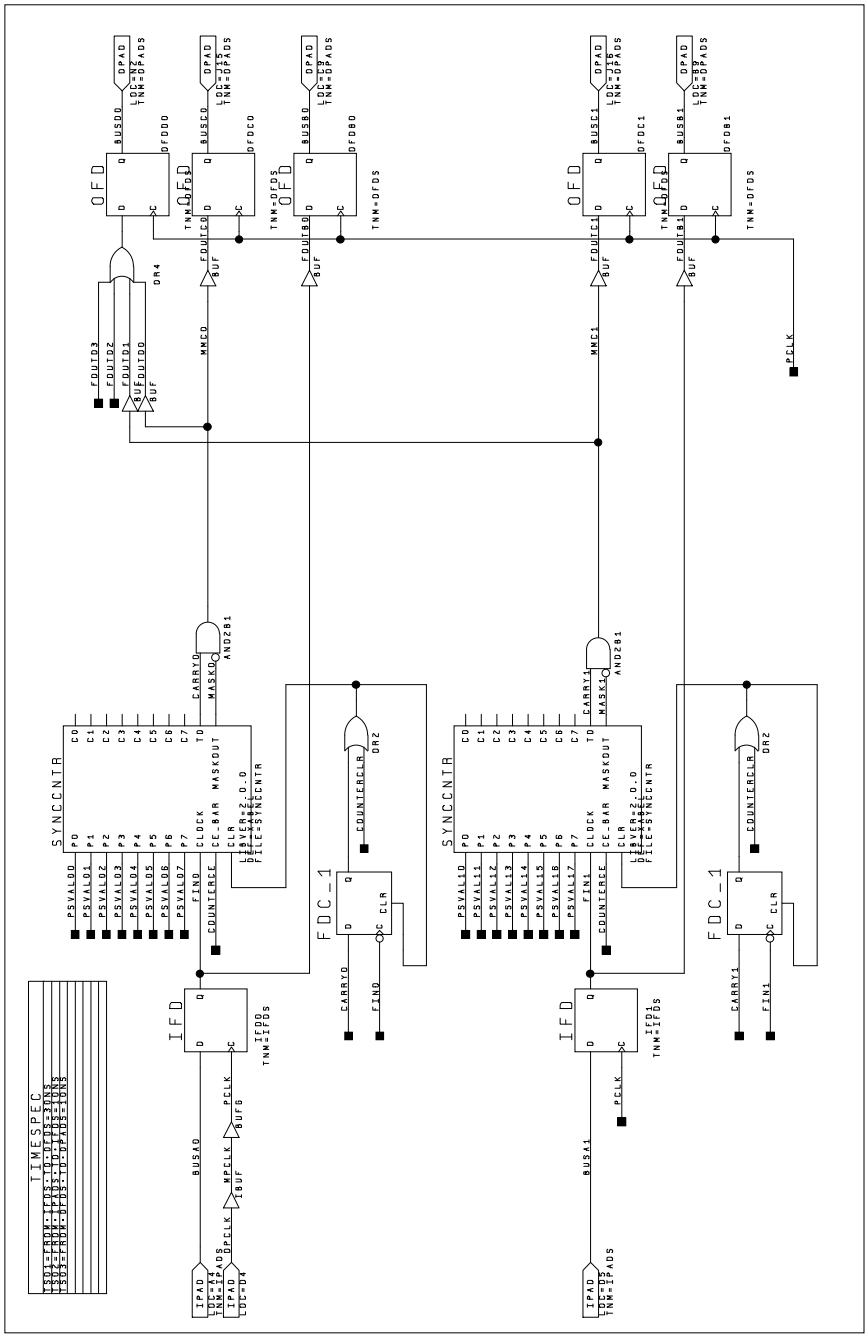


Figure B.9: The Prescale and Mask Logic (page 3)

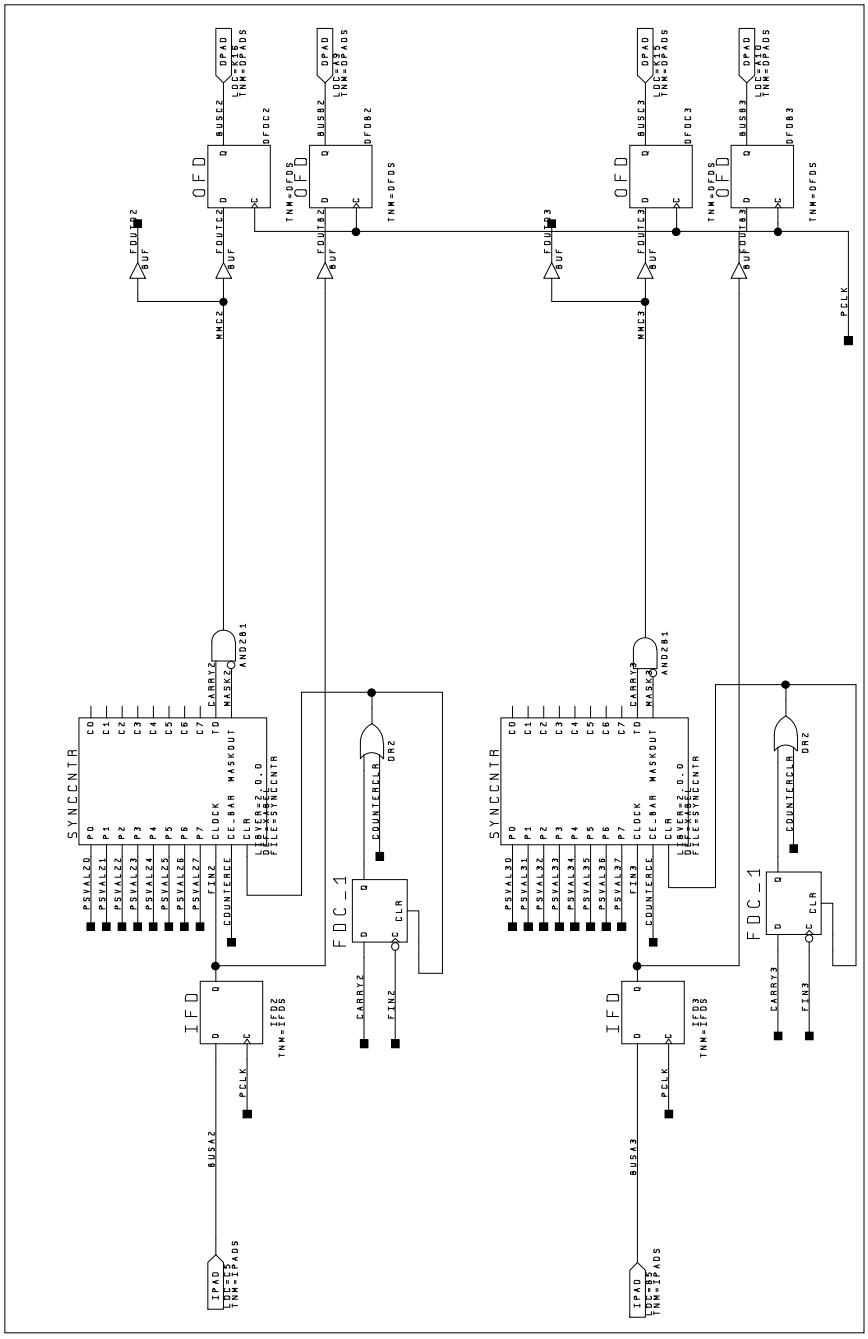


Figure B.10: The Prescale and Mask Logic (page 4)

```
"address
        SELECT = ((S32 # U32) & !MS0 & !MS1 & !MS2 # (S24 # U24) & !MS0 & !MS1) & !AS & IACK;

"address modifier
        S24 = (AMCODE==^h3E)#(AMCODE==^h3D);
        U24 = (AMCODE==^h3A)#(AMCODE==^h39);
        S32 = (AMCODE==^h0E)#(AMCODE==^h0D);
        U32 = (AMCODE==^h0A)#(AMCODE==^h09);

"data strobe
        RSL = WRITE & SELECT & !DS0;
        RSH = WRITE & SELECT & !DS1;
        WSL = !WRITE & SELECT & !DS0;
        WSH = !WRITE & SELECT & !DS1;

"250ns active delay
        DELAYIN = !DS0 # !DS1;

"data acknowledge / buss error
        BDTACK = !WRITE & SELECT & DLAY3 & (!DS0 # !DS1) # WRITE & SELECT & DLAY3 & (!DS0 # !
        BBERR = GND;

"74LS645
        DIR = RSL;              "1 for read operation

"addresss asignment
"256bit VME address space
        RSTAT   = SELECT & (ADDR == ^H00);
        WCTRL   = SELECT & (ADDR == ^H04);
        COMMAND = SELECT & (ADDR == ^H08);
        PROGX   = SELECT & (ADDR == ^H0C);
        TDITM   = SELECT & (ADDR == ^H10);

"i.e
"       0x00    STATUS REGISTER (R)
"       0X04    WRITE CONTROL REGISTER [Not Used]
"       0X08    COMMAND REGISTER (W)
"       0X0C    PROGRAM XILINX FROM VME enable[bit0 1=enable]
"       0X10    WRITE TMS[bit0] AND TDI[bit1]
"end of equations
"test vectors
"end of test vectors

END vme_t
```

B.0.4 Fan out

Figures B.15, B.16, B.17 are the electric schematic of the Fan Out board.

B.0.5 TIMS

Figures B.18, B.19, B.20 are the electric schematic of the TIMS board.

B.0.6 RFCG

Figures B.21, B.22 are the electric schematic of the RFCG board.

B.0.7 Scaler

Figure B.23 is the ViewLogic schematic of the Scaler. This is for one of the four chips. It counts the number of signals which are not vetoed. The design of the scaler to count regardless to the veto signal is almost same; just always enabling the counter. Bellow is the XAbel source file, which is used as the symbol "ADEC1" in the Scaler. This logic is developed by N.Mizutani.

```
module ADEC1
title   '4bit address decoder for Suehiro module
                  16 Sep. 1997   MIZUTANI Natsuko'

declarations
"Input Pins
        A4,A3,A2,A1                     pin;
"Output Pins
        AEQ15,AEQ14,AEQ13,AEQ12         pin;
        AEQ11,AEQ10, AEQ9, AEQ8         pin;
         AEQ7, AEQ6, AEQ5, AEQ4         pin;
         AEQ3, AEQ2, AEQ1, AEQ0         pin;
"Logic Levels
        H,L,VCC,GND,X,Z,C = 1,0,1,0,.X.,.Z.,.C.;
"vector definitions
        ADDRESS = [A4..A1];

equations
        AEQ0  = (ADDRESS == 0);
        AEQ1  = (ADDRESS == 1);
        AEQ2  = (ADDRESS == 2);
        AEQ3  = (ADDRESS == 3);
        AEQ4  = (ADDRESS == 4);
        AEQ5  = (ADDRESS == 5);
```

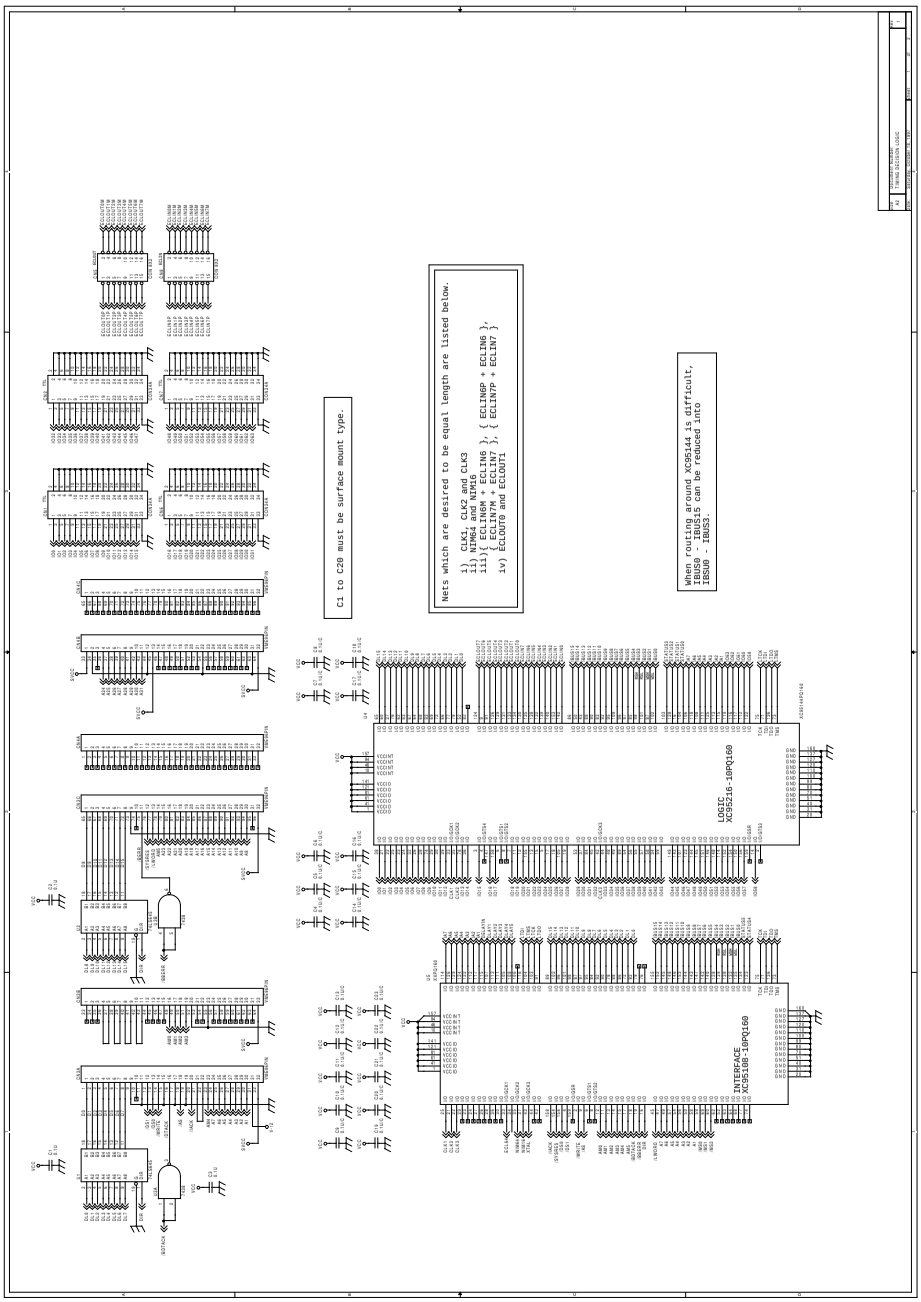


Figure B.11: The Timing Decision Logic Board (page 1)

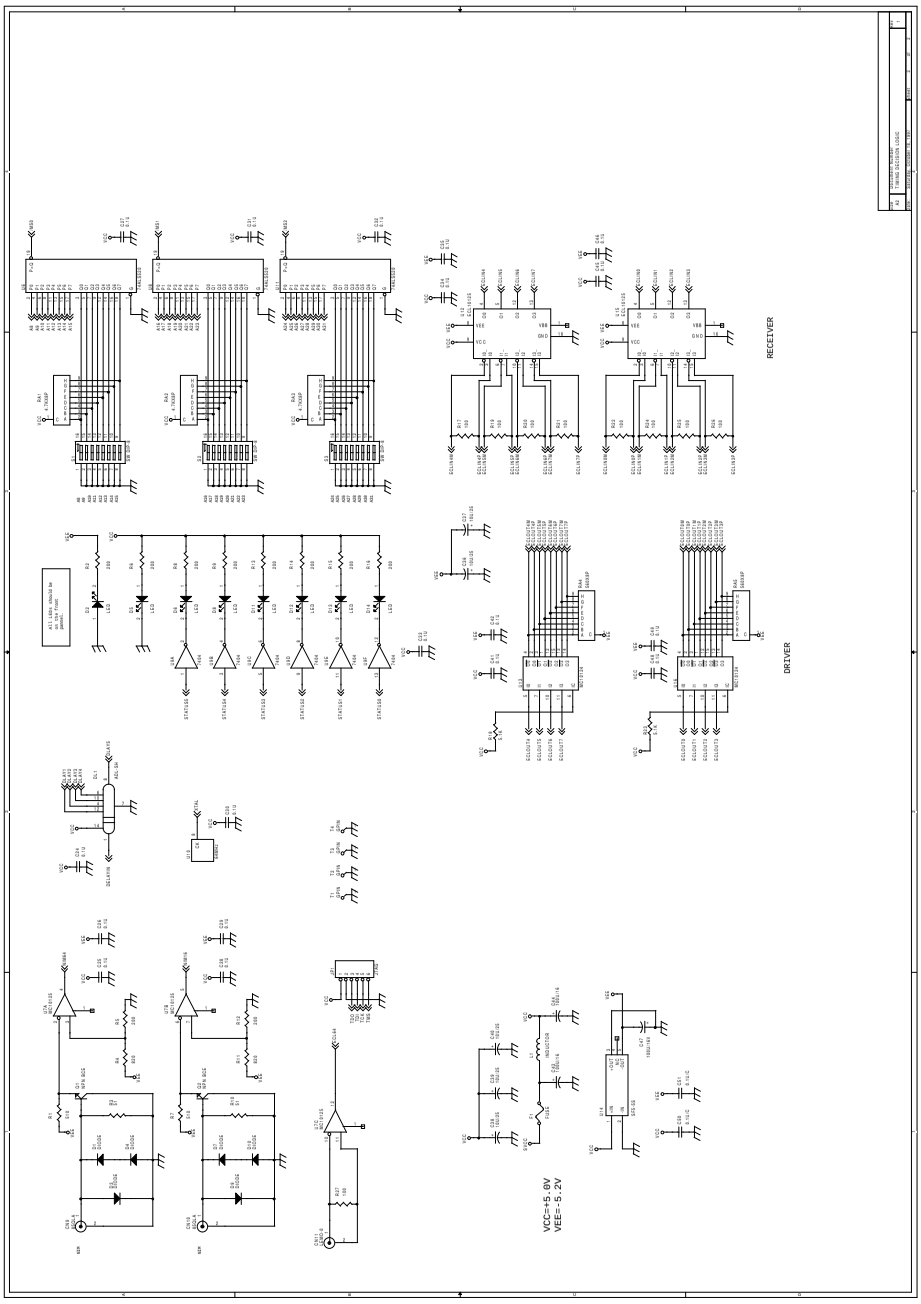


Figure B.12: The Timing Decision Logic Board (page 2)

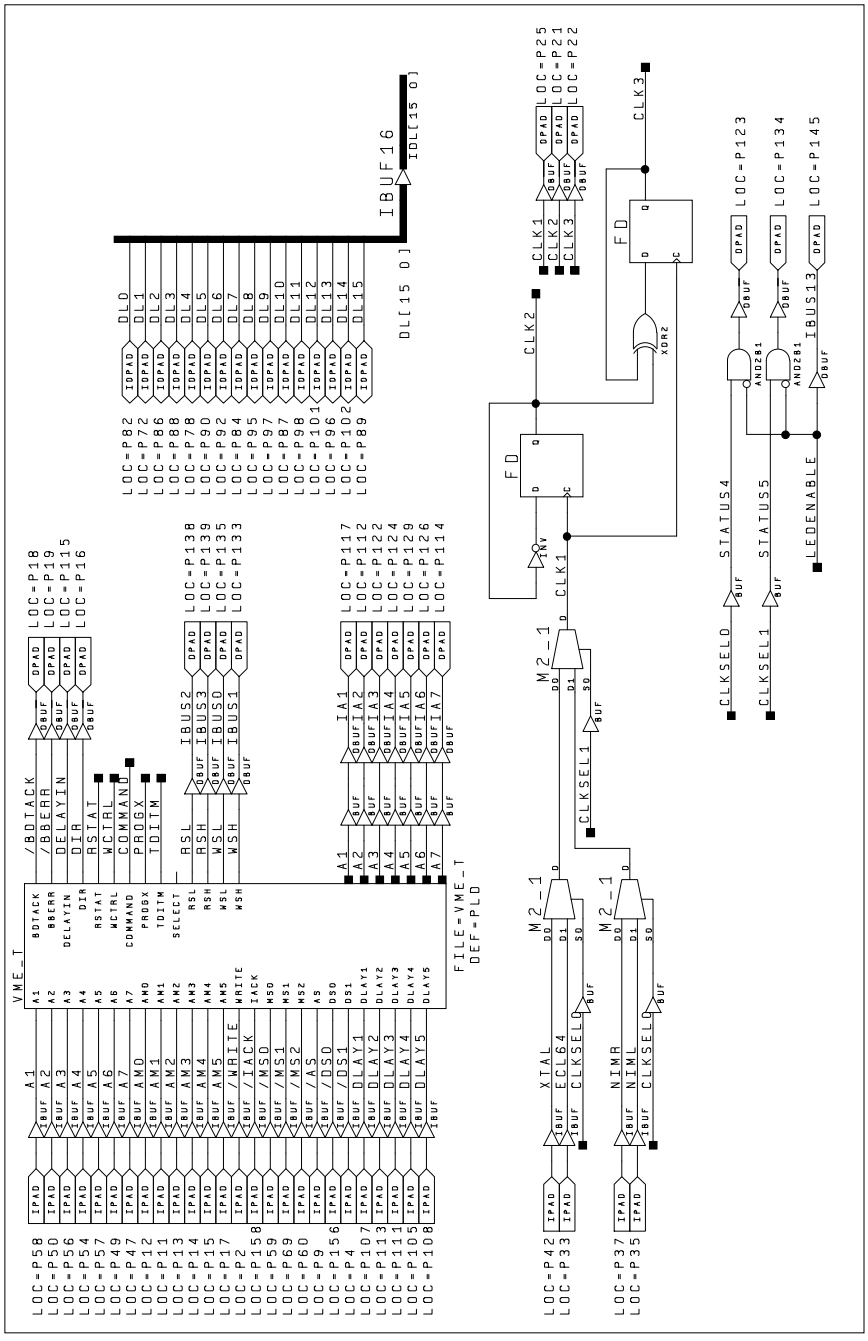


Figure B.13: The VME interface part of Timing Decision Logic Board (page 1)

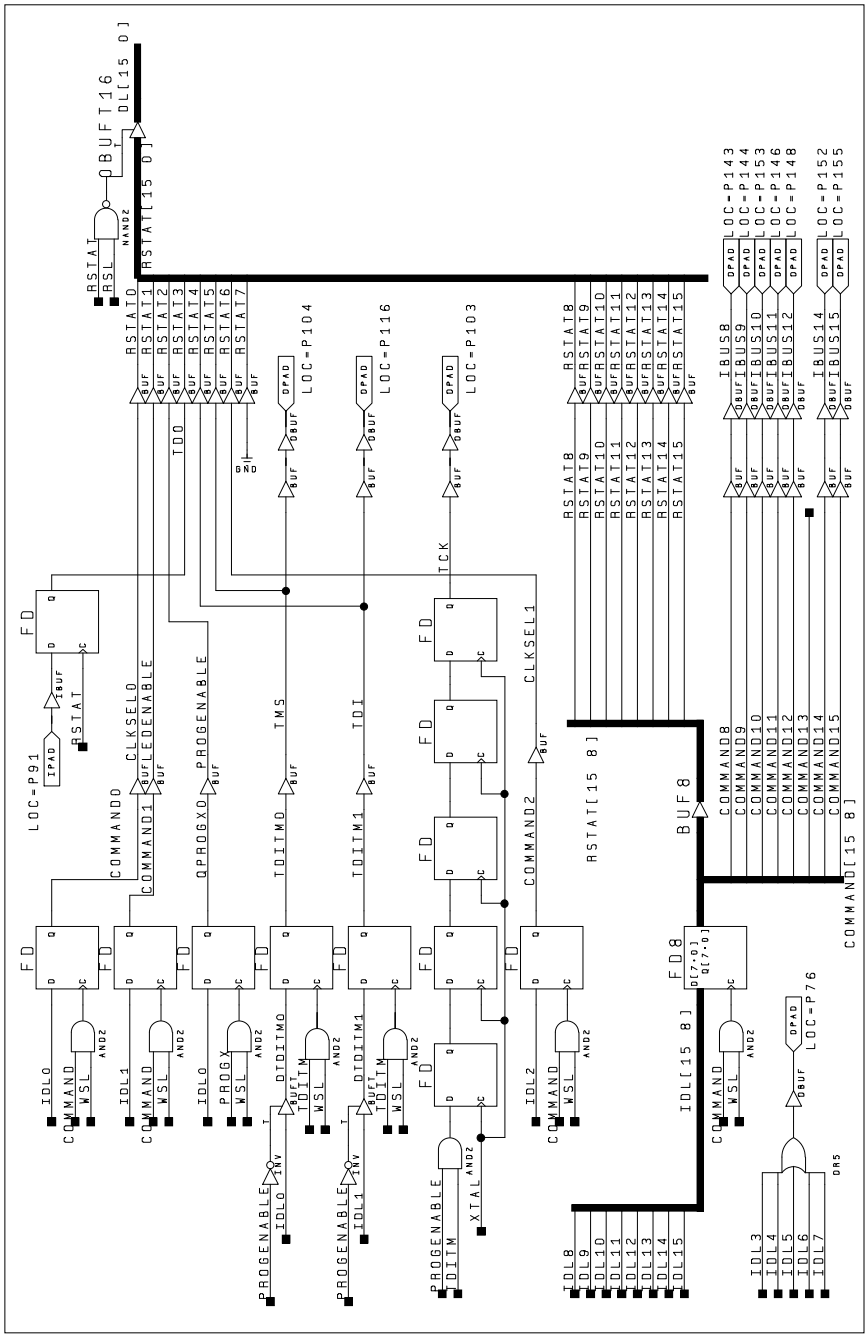


Figure B.14: The VME interface part of Timing Decision Logic Board (page 2)

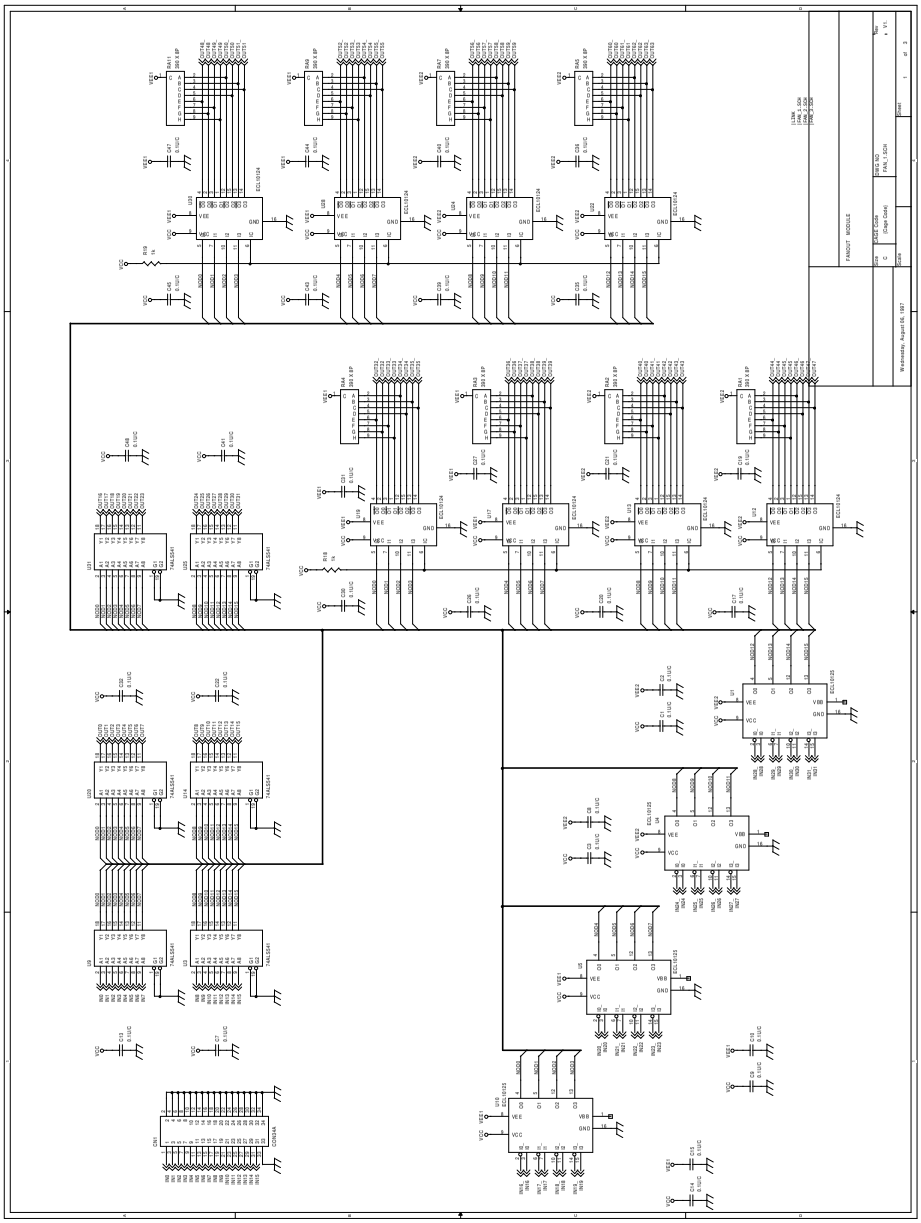


Figure B.15: The Fan Out Board (page 1)

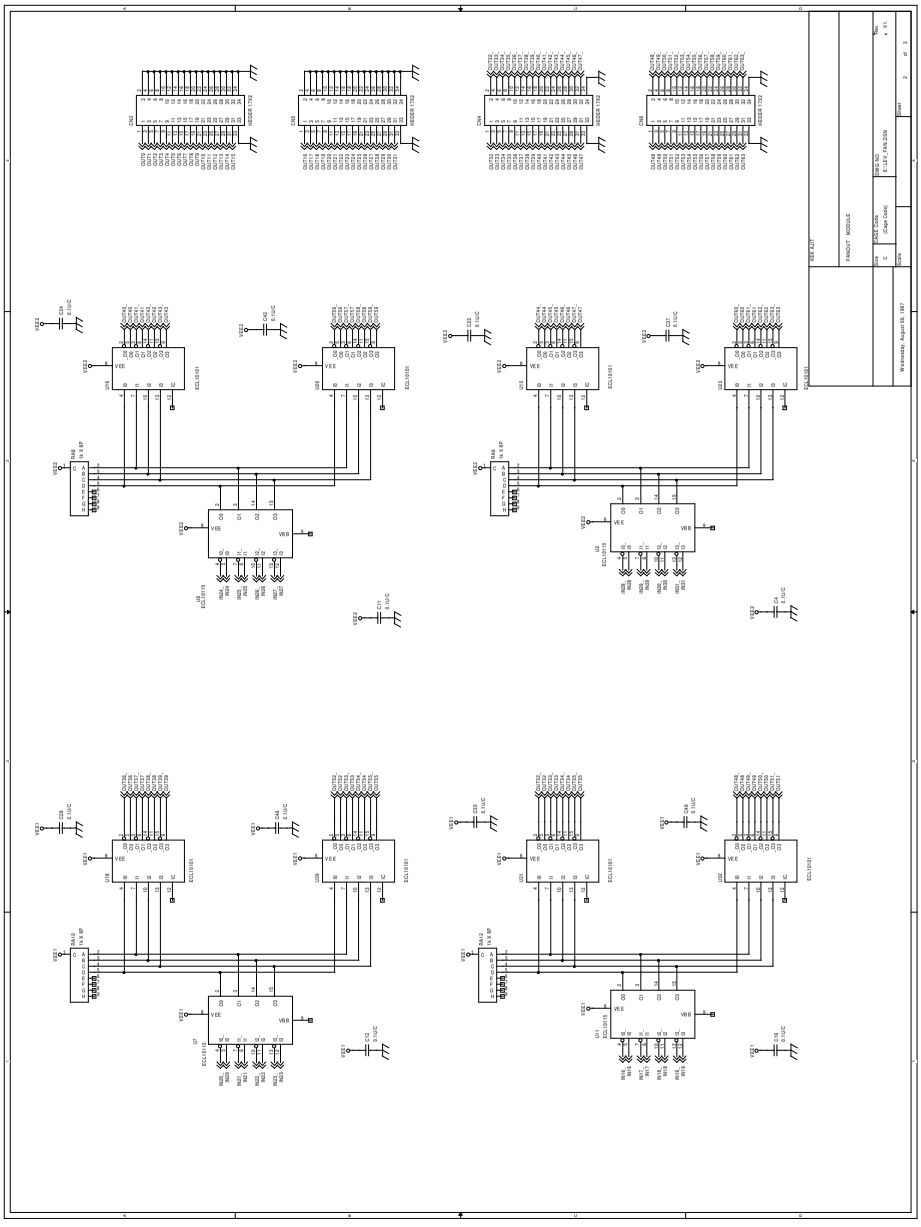


Figure B.16: The Fan Out Board (page 2)

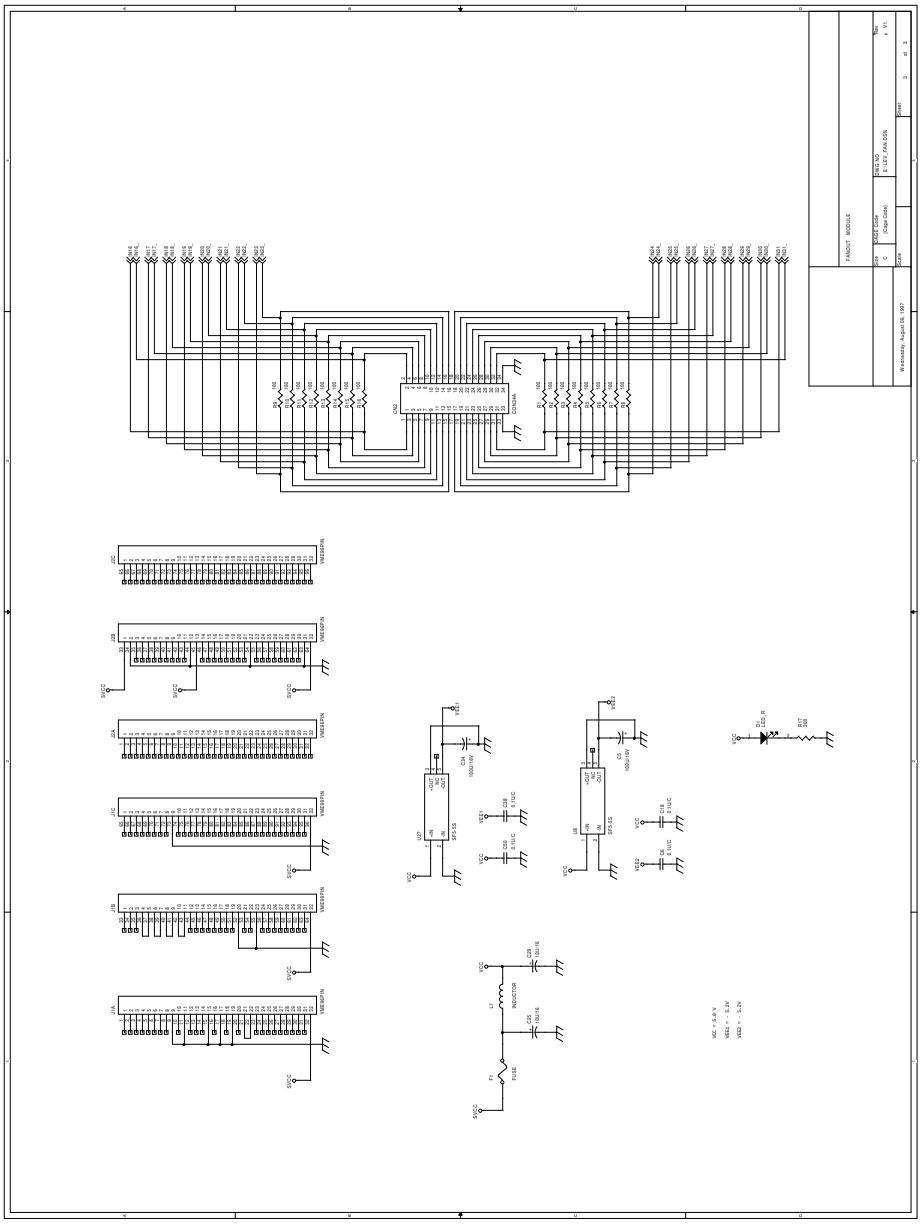


Figure B.17: The Fan Out Board (page 3)

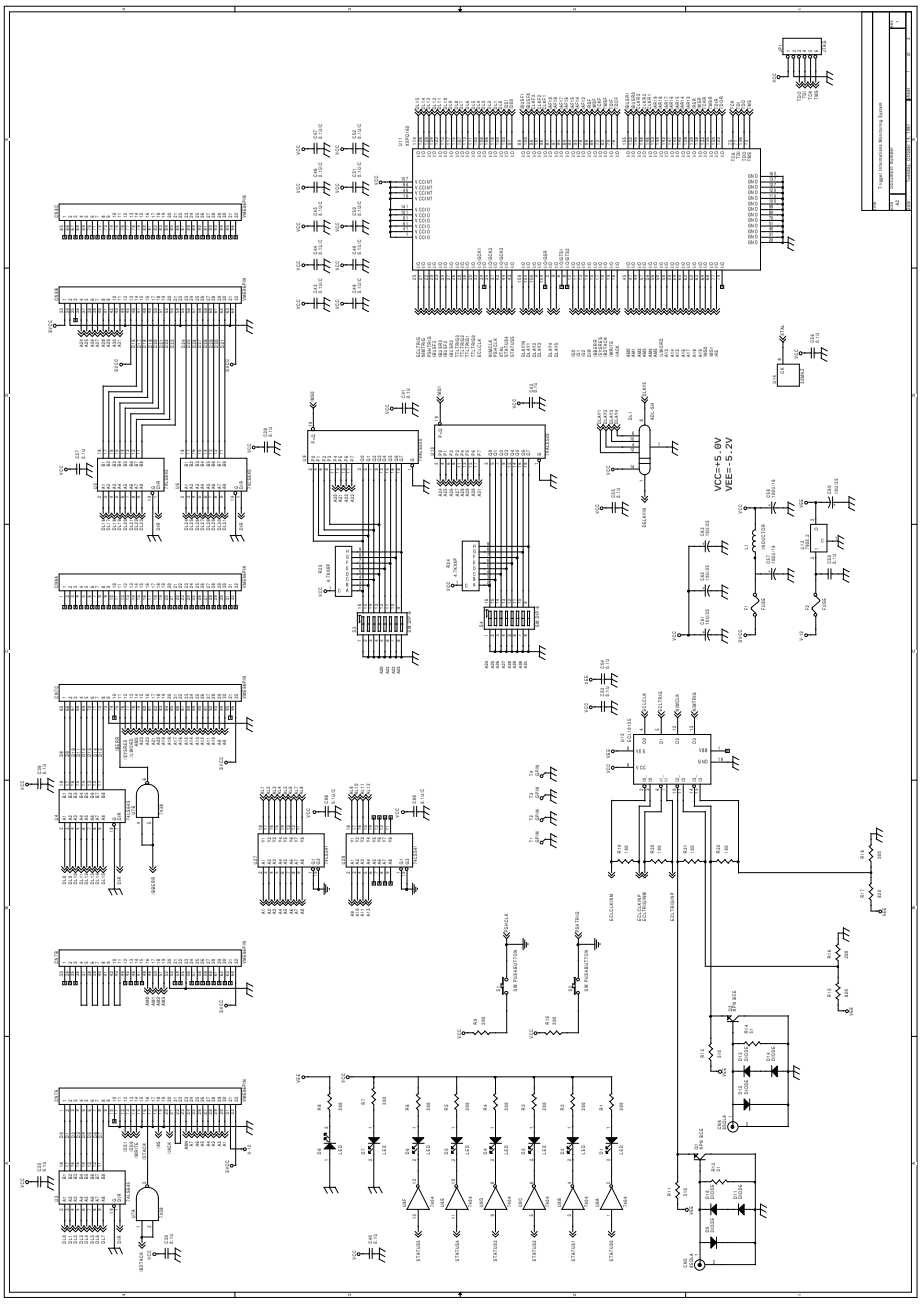


Figure B.18: The Trigger Information Monitoring System Board (page 1)

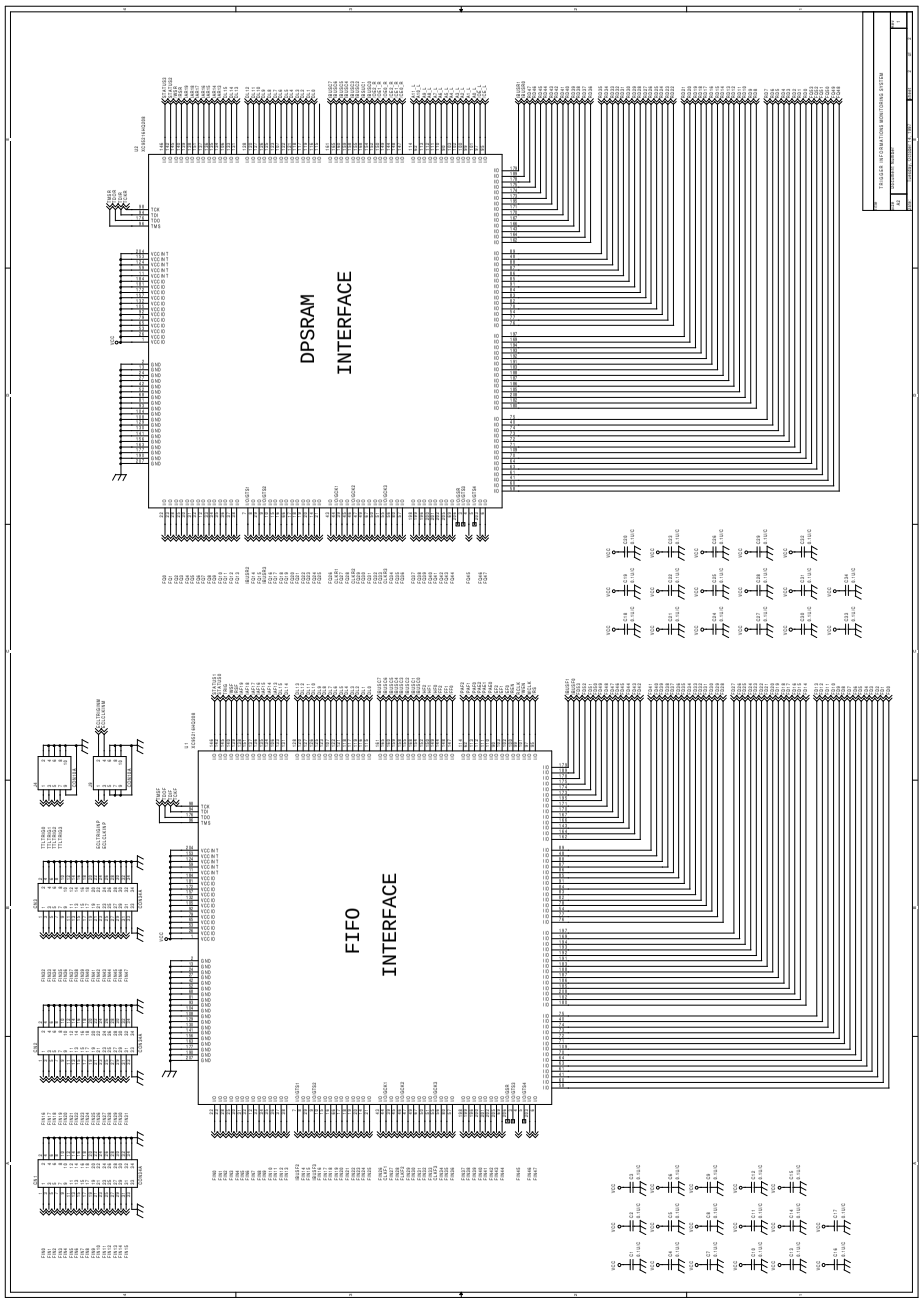


Figure B.19: The Trigger Information Monitoring System Board (page 2)

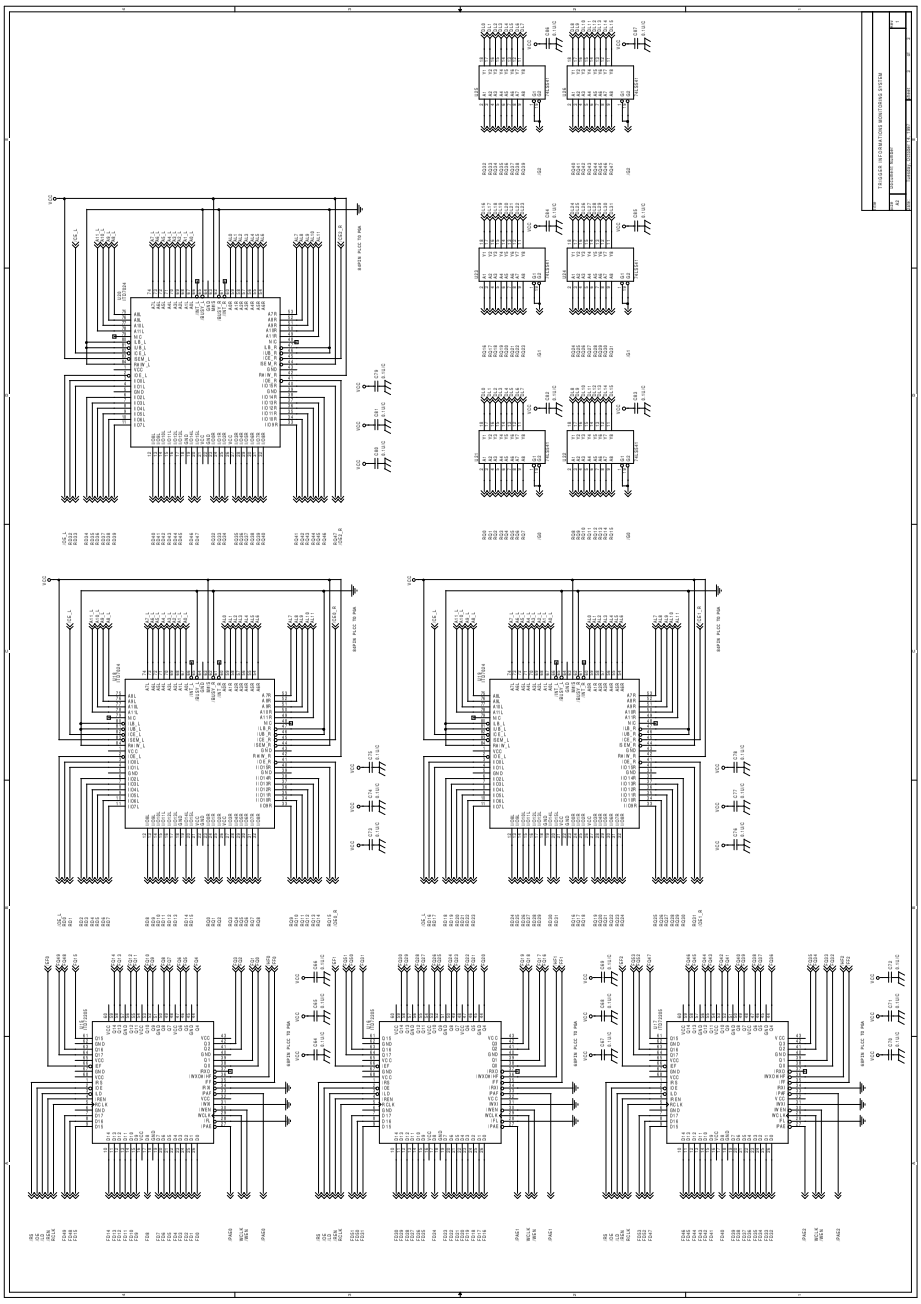


Figure B.20: The Trigger Information Monitoring System Board (page 3)

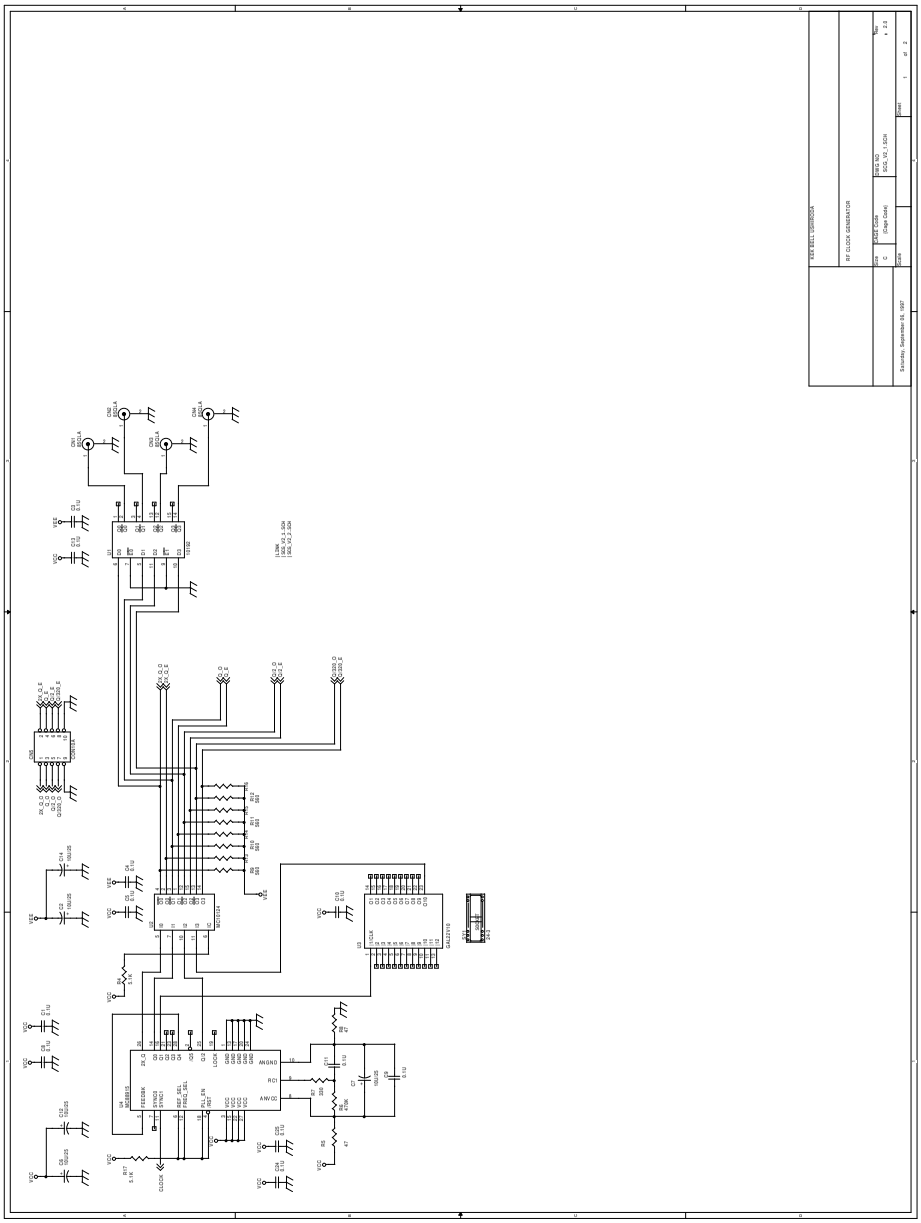


Figure B.21: The RF Clock Generator Board (page 1)

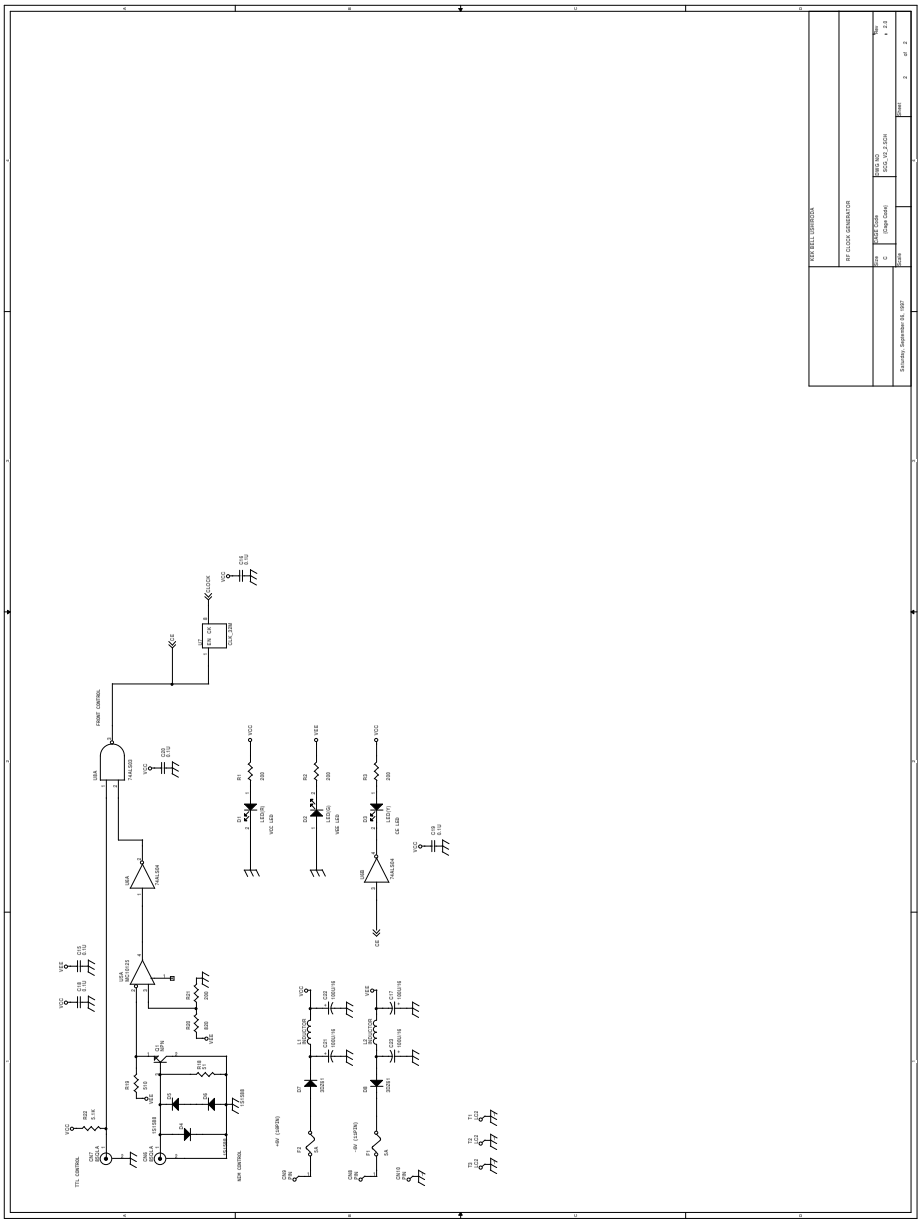


Figure B.22: The RF Clock Generator Board (page 2)

```
        AEQ6  = (ADDRESS == 6);
        AEQ7  = (ADDRESS == 7);
        AEQ8  = (ADDRESS == 8);
        AEQ9  = (ADDRESS == 9);
        AEQ10 = (ADDRESS ==10);
        AEQ11 = (ADDRESS ==11);
        AEQ12 = (ADDRESS ==12);
        AEQ13 = (ADDRESS ==13);
        AEQ14 = (ADDRESS ==14);
        AEQ15 = (ADDRESS ==15);

test_vecrtors ( [A1,A2,A3,A4]->[AEQ0,AEQ1,AEQ2,AEQ3] )
[0,0,0,0]->[1,0,0,0];
[1,0,0,0]->[0,1,0,0];
[0,1,0,0]->[0,0,1,0];
[1,1,0,0]->[0,0,0,1];

end ADEC1
```

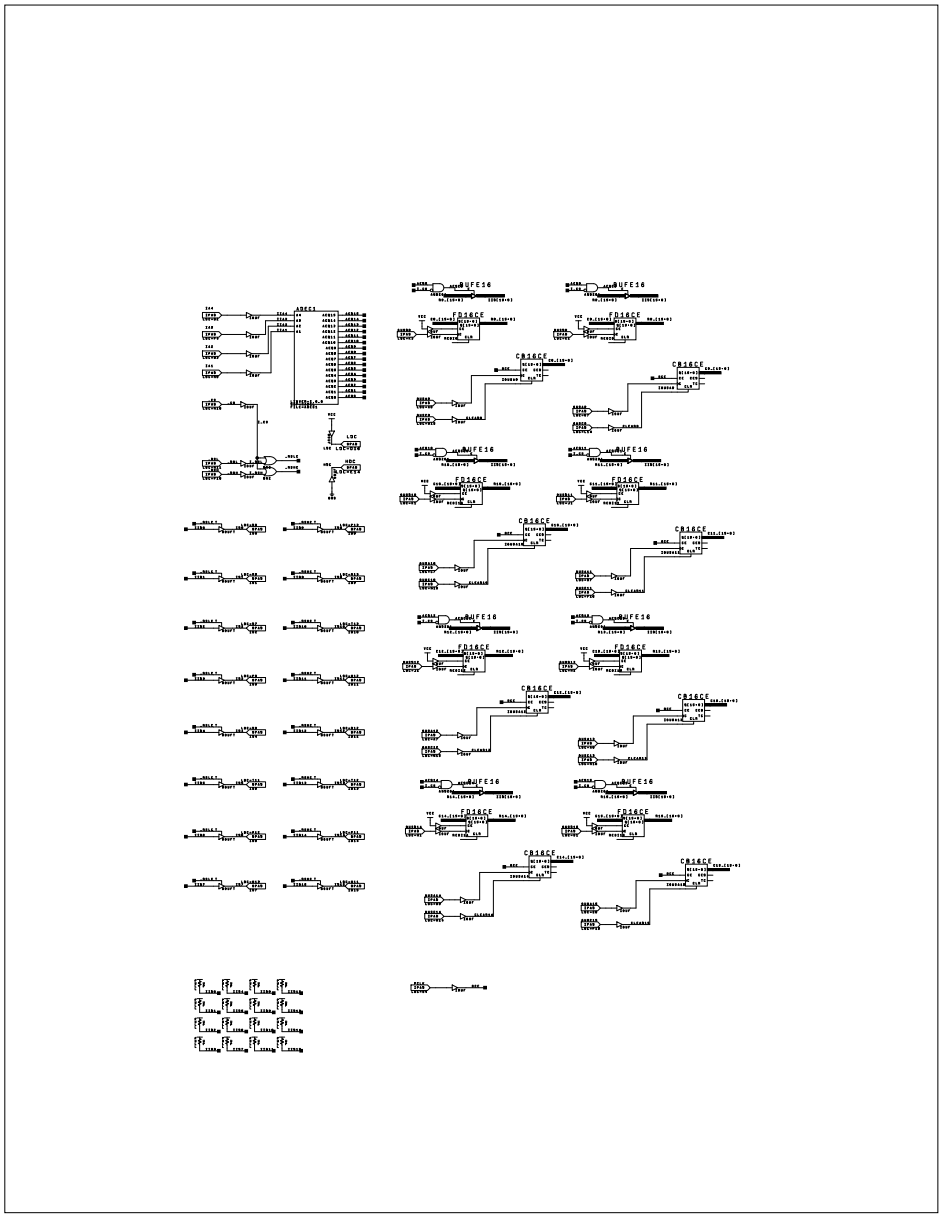
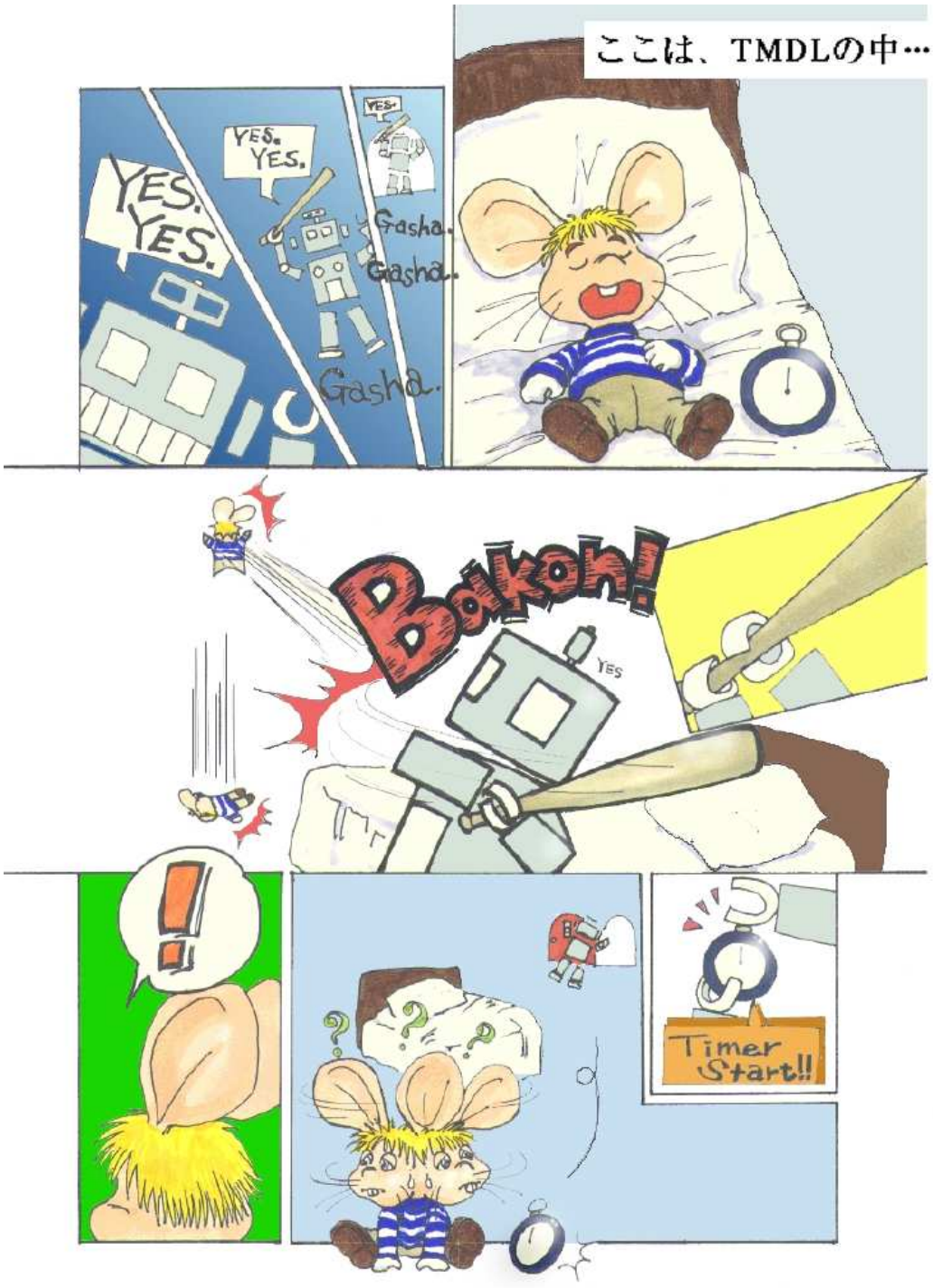


Figure B.23: The Scaler

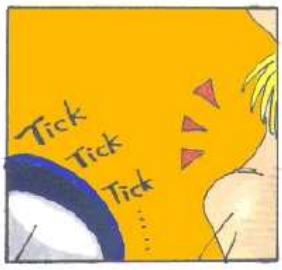
Appendix C

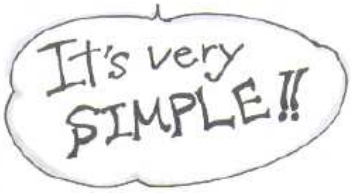
Cartoon "How to Assert the Final Trigger"

This cartoon explains the way how to assert the final trigger of BELLE. This was favorably received by those who don't want to follow the complecated logic of GDL (TMDL). In this cartoon, the cue signal is called "LOGICYES", a robot. Note that the order to read is the Japanese way, i.e. the upper-right to the lower-left. The cartoon was planned by me and drawn by M.Yokoi with help of M.Sasaki.

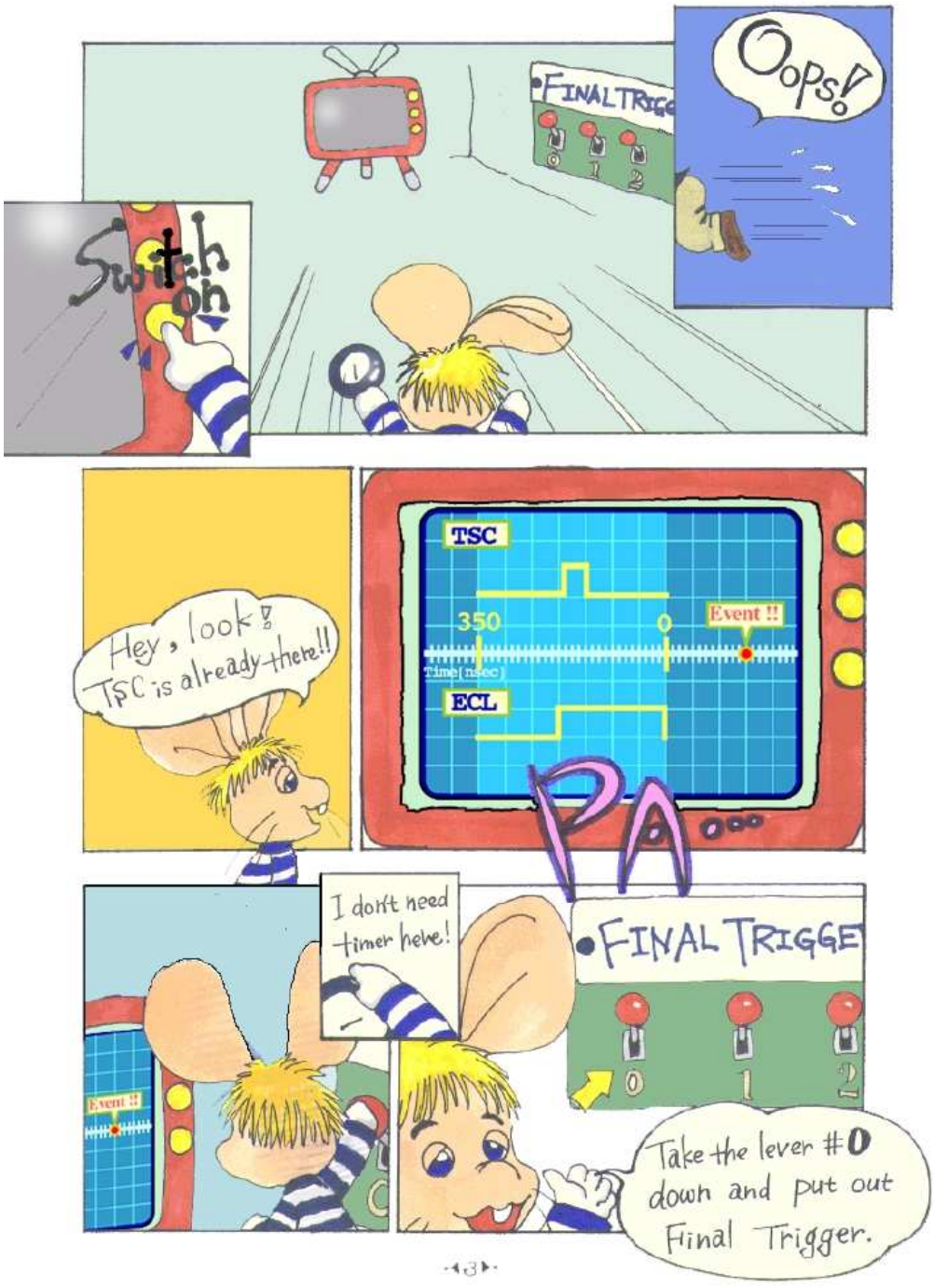

ここは、TMDLの中…
YES. YES.
YES. YES.
YES.
Gasha.
Gasha.
Gasha.
Bokoh!
YES
!
Timer Start!!

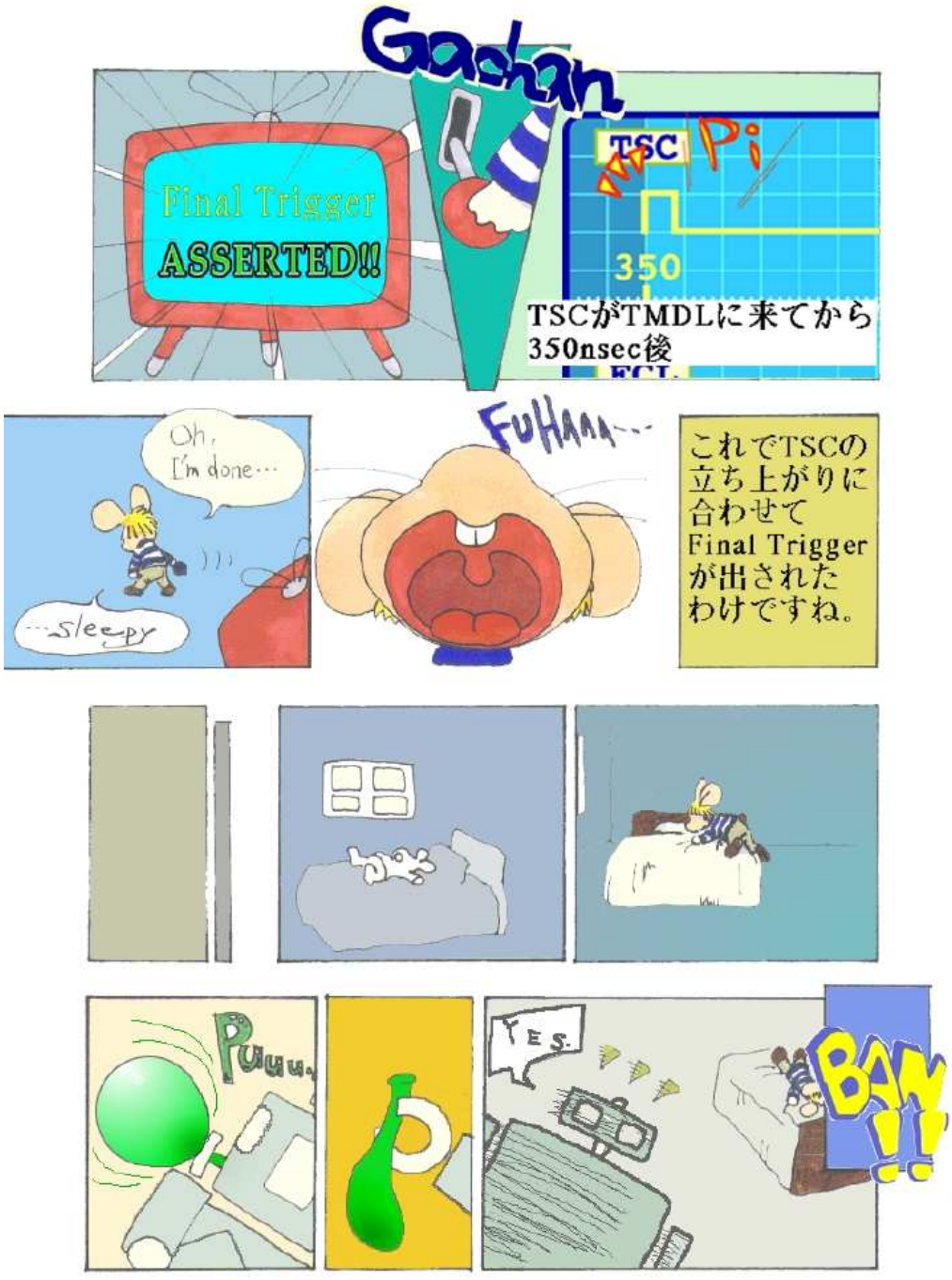
HOW TO ASSERT FINAL TRIGGER

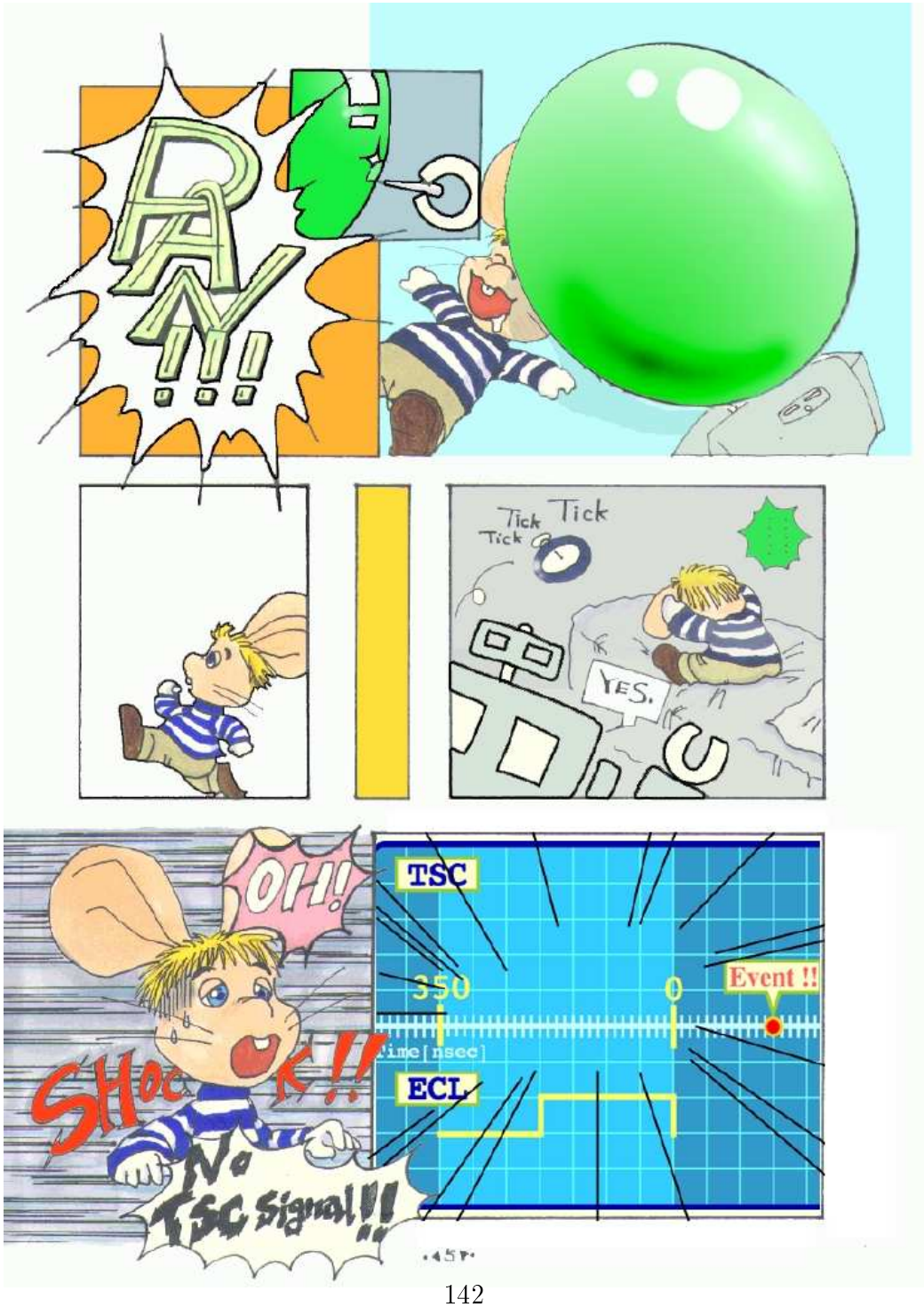




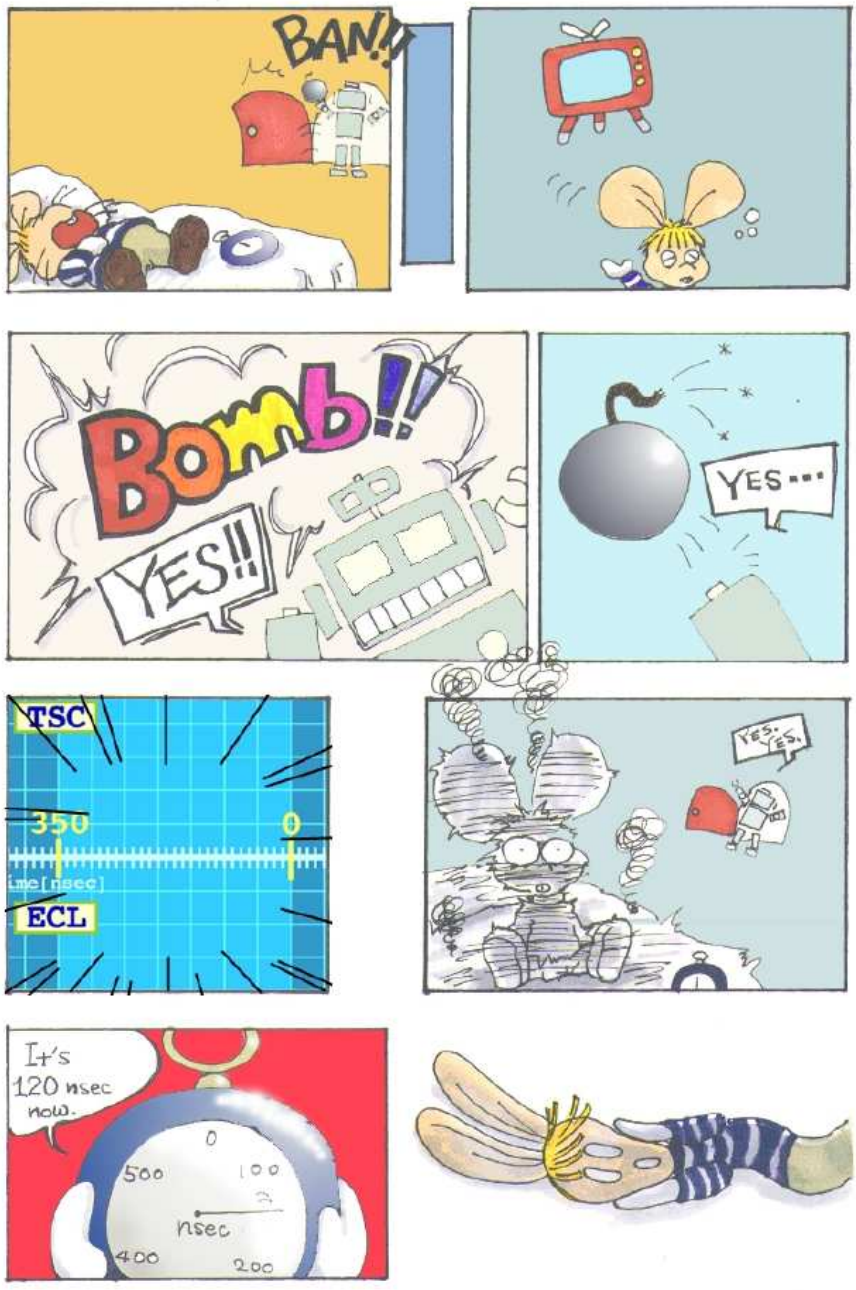
お昼寝中のUsshyは、LOGICYESくんにたたき起こされてしまいました。
さぁ、これから何が起こるのかな？？

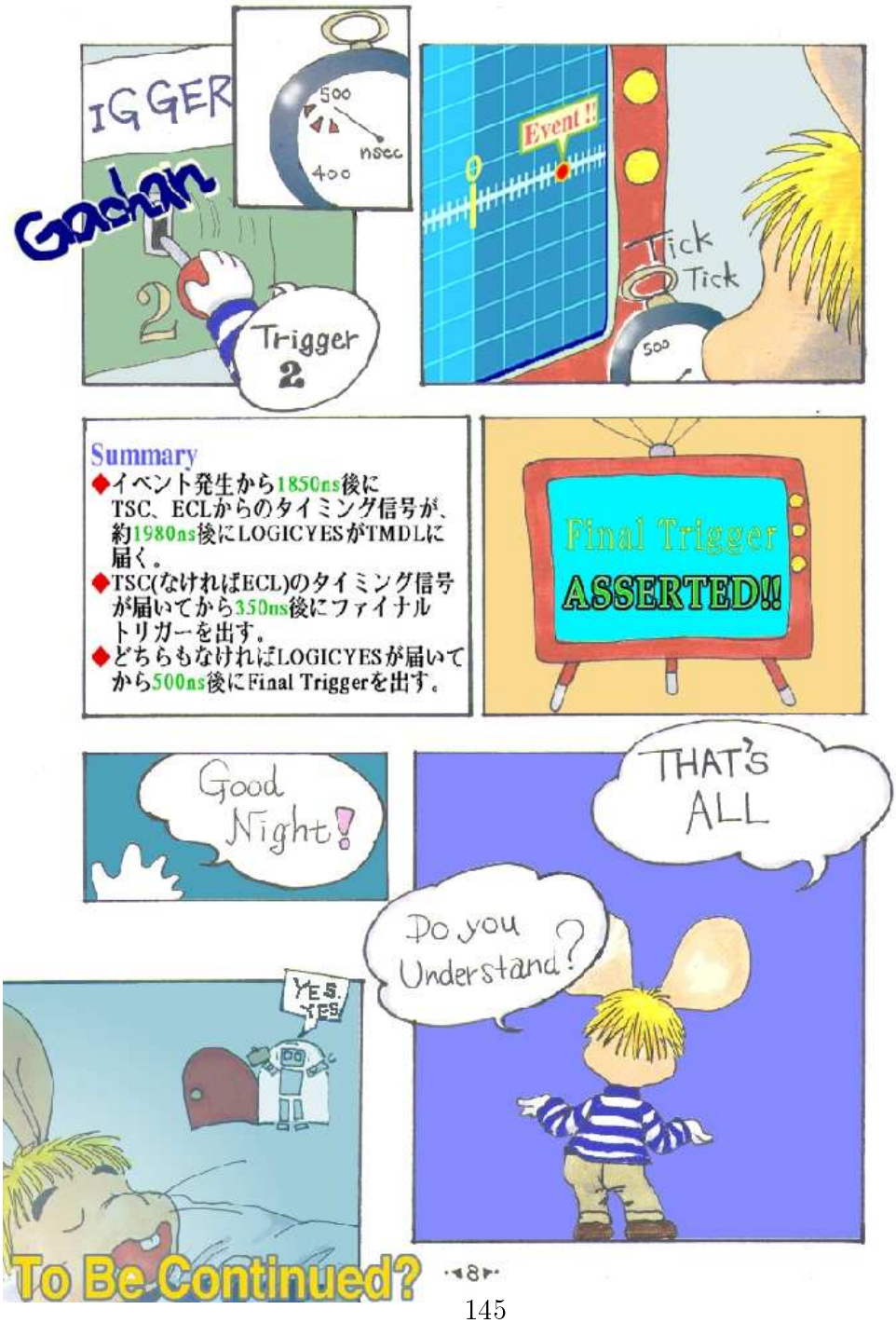

Switch on
FINAL TRIGG
0 1 2
Oops!
Hey, look! TSC is already there!!
TSC
350
0
Event !!
Time (nsec)
ECL
PA...
I don't need timer here!
FINAL TRIGGE
0 1 2
Event !!
Take the lever #0 down and put out Final Trigger.


Gaahan
Final Trigger
ASSERTED!!
TSC
Pi
350
TSCがTMDLに来てから
350nsec後
ECL
Oh,
I'm done…
…sleepy
FUHAAA…
これでTSCの
立ち上がりに
合わせて
Final Trigger
が出された
わけですね。
Puuu.
YES.
BAN!!


RAN!!!
Tick
Tick
Tick
YES.
OH!
SHOCK!!
No TSC Signal!!
TSC
350
0
Event !!
Time[nsec]
ECL

ECL
Pi…
adjusting to the ECL leading edge,
ECL
In Such case
Gachan
take the lever #1 down
たんじゅんに。
でも、もし…
途中でTSCが姿を現したら…
inal Trigger
SSERTED!!
It's O.K.!!
どうして TSCがいいのかな？
TSC is more precise and reliable
in timing than ECL
TSCに合わせて
Lever #0
TSC arrived!!
Take it. It's precise


BAN!!
Bomb!!
YES!!
YES...
TSC
350
0
ime[nsec]
ECL
YES. YES.
It's
120 nsec
now.
0
500
100
nsec
400
200


IGGER
Gaelan
500
nsec
400
2
Trigger
2
Event !!
Tick
Tick
500
Summary
◆イベント発生から1850ns後に
TSC、ECLからのタイミング信号が、
約1980ns後にLOGICYESがTMDLに
届く。
◆TSC(なければECL)のタイミング信号
が届いてから350ns後にファイナル
トリガーを出す。
◆どちらもなければLOGICYESが届いて
から500ns後にFinal Triggerを出す。
Final Trigger
ASSERTED!!
Good
Night!
THAT'S
ALL
Do you
Understand?
YES.
YES
To Be Continued?

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